Appendix 2 v7

EUROPEAN PARTNERSHIP

APPENDIX 2: ACTIVITIES LAUNCHED IN 2023 FOR THE INITIATIVE PART

DECISION CHIPS GB 2023.51

Amending the Chips JU work programme for the year 2023

THE GOVERNING BOARD OF THE CHIPS JOINT UNDERTAKING

Having regard to Council Regulation (EU) 2023/1782 of 25 July 2023 amending Council Regulation (EU) No 2021/2085 of 19 November 2021 establishing the Joint Undertakings under Horizon Europe (hereinafter "Single Basic Act") and in particular Articles 3(4), Article 5(2)(q), Article 17(2)(k) and Article 17(2)(b1) thereof;

Having regard to the Public Authorities Board's opinion on the work programme for the year 2023 in accordance with Article 19(4)c;

Having regard to GB decision 2023.37 amending the work programme 2023;

WHEREAS:

1) The Executive Director shall prepare and, after having taken into account the opinion of the PAB, submit for adoption by the Governing Board the work programme and the corresponding expenditure estimates;

2) With the entry into force of the Chips Act on 21 September 2023, the Chips for Europe Initiative ('Initiative') has been established. The Initiative is composed of the following five components: Setting up a Design Platform; Enhancing existing and developing new advanced pilot lines; Building capacities for accelerating the development of Quantum chips and associated semiconductor technologies; Establishing a network of competence centres across the Union; and Setting up a Chips Fund to facilitate access to debt financing and equity, in particular for start-ups, scale-ups, SMEs and small mid-caps.;

3) With the exception of the Chips Fund, the other four components will be implemented by the Chips Joint Undertaking;

4) The work programme 2023 should be amended to include the second component on pilot lines. These pilot lines will have the purpose of process development, test and experimentation, as well as small-scale production. They will serve as a platform for European research and development with an industrial perspective to bridge the gap between the Union's advanced research and innovation capabilities and their sustainable industrial exploitation;

5) Given the strategic importance to bridge this gap and the direct impact this has on the EU's strategic autonomy and technological sovereignty, the Chips Joint Undertaking should co-own 50% of the tools and equipment that constitute the pilot lines. This will allow the Chips Joint Undertaking to keep a closer control over such strategic infrastructures, thereby making future reporting exercises towards auditing authorities more transparent and straightforward;

6) To this end, the Governing Board should adopt, as annexes to this work programme, four Calls for Expression of Interest (CfEoI) with the objective of selecting Hosting Consortia that will implement pilot lines on '*Advanced sub 2nm leading-edge system on chip technology*'; '*Advanced Fully Depleted Silicon On Insulator technologies targeting 10 to 7nm*'; '*Advanced Packaging and Heterogenous Integration*'; and '*Novel materials for advanced semiconductor devices*'. The Governing Board should assign the task of launching these Calls to the Public Authorities Board;

7) The budget of the Chips Joint Undertaking has been updated to provide funding to these components (decision GB 2023.48);

HAS ADOPTED THIS DECISION:

Article 1

The amendment to work programme 2023, as annexed to this decision, is hereby adopted.

It shall be published on Chips Joint Undertaking's website.

Article 2

This Decision shall enter into force on the date of its adoption.

Done in Brussels, on 1st December 2023

Ralf Bornefeld

Chair of the Governing Board

Annex: Amended work programme for the year 2023

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1. INTRODUCTION

This amendment to the work programme 2023 (WP2023) of the Key Digital Technologies (KDT), renamed Chips Joint Undertaking (Chips JU) as per Council Regulation (EU) 2023/1782 of 25 July 2023, covers new activities of the Chips JU for 2023 fulfilling the objectives of the Chips JU under the Chips for Europe Initiative ("Initiative"). The original WP2023 then covers the activities under the "non-Initiative" part of the programme.

The activities to be launched in this amendment stem from Article 126.2.(h) SBA, which read as follows:

"*enhance existing and develop new advanced pilot lines across the Union to enable development and deployment of cutting-edge semiconductor technologies and next-generation semiconductor technologies*;"

2. WORK PROGRAMME 2023 INITIATIVE PART

This amendment of the WP2023 foresees the launch of **four Calls for Pilot Line** (CPL) with an estimated EU expenditure of up to **EUR 1670 million**.

A Call for Pilot Line includes three interrelated calls:

- Call for Expression of Interest for the selection of a Hosting Consortium
- Call for proposals for Set-up, integration and process development, funded under the Horizon Europe Programme
- Call for proposals for the operational activities of the pilot line, funded under the Digital Europe Programme

whereby the same application is submitted to those calls. The evaluation of a CPL will consist of the simultaneous evaluation of the three interrelated calls. A consortium will only be eligible for funding if its proposal for all three calls passes the necessary thresholds.

The amendment describes the details of the call: topic description and the budgets as well as the procedures for evaluation and selection.

The selection of a proposal in a CPL then leads to the signature of a Hosting Agreement, one or more joint procurement agreements (JPAs) and a number of grant agreements. These joint procurements and grants will make use of multi-annual instalments.

2.1 Calls for pilot lines: EU and national budget

In 2023, the Chips JU will launch four CPL with the following **maximum EU expenditure**:

Action	Title	Maximum EU Expenditure (M€)
Chips 2023-CPL-1	Advanced sub 2nm leading-edge system on chip technology	700.00
Chips 2023-CPL-2	Advanced Fully Depleted Silicon On Insulator technologies targeting 7nm	420.00
Chips 2023-CPL-3	Advanced Packaging and Heterogenous Integration	370.00
Chips 2023-CPL-4	Advanced semiconductor devices based on Wide Bandgap materials	180.00
	Total	1670.00

National commitments:

	2023 I
AT	14.500.000,00
BE	750.000.000,00
BG	
CY	
CZ	
DE	373.320.000,00
DK	
EE	
EL	650.000,00
ES	1.000.000,00
FI	49.829.000,00
FR	383.300.000,00
HR	
HU	
IE	20.000.000,00
IL	
IS	
IT	106.000.000,00
LV	
LU	
LT	
MT	
NL	
NO	
PL	28.000.000,00
PT	17.650.000,00
RO	5.000.000,00
SE	13.750.000,00
SK	
SI	
TR	
PS commitments	1.762.999.000,00
EU commitment	1.670.000.000,00

Reimbursement rate for establishing the EU contribution

Reimbursement rate as percentages of the eligible costs

- EU contribution as % of the eligible cost according to Horizon Europe (*): up to 100%
- EU contribution as % of the eligible cost according to Digital Europe (*): up to 50%

(*) beneficiaries may ask for a lower contribution

The EU budgets above will be matched by national contributions.

The next chapters cover:

3. Technical description of the topics
4. Description of the CPL including annexes

Under annexes several drafts and templates are provided for different documents, which can be modified to fit the specificities of the different pilot lines.

2.2 Specific provisions applicable to Calls for pilot lines

The following points on access conditions, Intellectual Property, and co-ownership apply to all Calls for pilot lines. More detailed provisions are stated in the Call for Pilot Line part of this document; in case of conflicts, those provisions prevail over the provisions stated here.

Access conditions for pilot lines

Expressions of Interest submitted to the calls below need to take into account the following access conditions:

- Access to a pilot line needs to be open to a wide range of public and private users across the Union and granted on a transparent and non-discriminatory basis directly proportional to the financial contribution by the Union to the total costs of those activities
- Access needs to be provided on market terms, or on a cost-plus-reasonable-margin basis for large undertakings, while granting preferential access or reduced prices for academic institutions, start-ups and SMEs
- PDKs/ADKs need to be accessible for different categories of users (academia, research, industry etc.) and will be required to be available via the European virtual Design Platform.

- Access conditions for non-EU organisations need to take into account the Union's commitments to international cooperation under its strategic partnerships with like-minded countries.

Intellectual Property

Expressions of Interest submitted to the calls below need to take into account the following provisions on Intellectual Property:

- Intellectual Property provisions must comply with standard Horizon Europe and Digital Europe rules. For instance, IPR transfers to legal entities outside the EU will be subject to approval by the granting authority.
- However, any transfer of IP rights from the hosting consortium to any third parties needs to be tied to either potential investment in Europe or an international agreement.
- Possible conditions for non-exclusive licensing of IP need to be considered.
- Consortia are invited to further reflect on the impact of EU co-ownership on IP policy.

Co-ownership

The ownership share of the Chips Joint Undertaking of the acquired equipment infrastructure in a pilot line is 50%.

2.3 Other general provisions

1. **Gender dimension**
   The integration of the gender dimension (sex and gender analysis) in research and innovation content is not a mandatory requirement. However, activities concerning user interaction or sensing (e.g. of medical devices, consumer goods, cars with automatic driving features, ...) need to include (if relevant) considerations of how the gender dimension affects system design, and hence whether it affects the technical specifications.
2. **Financial capacity**
   In line with the Financial Regulation, coordinators will be invited to complete a self-assessment using an on-line tool.
3. **Consortium agreement**: Participants are required to conclude a consortium agreement. For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.
4. **Costs for the pilot line** can be introduced as of the day after the publication date of the Call for Pilot Line.
5. For the purposes of the eligibility conditions, applicants established in Horizon Europe Associated Countries or in other third countries negotiating association to *Horizon Europe will be treated as entities established in an Associated Country, if the Horizon Europe*

association agreement with the third country concerned applies at the time of signature of the grant agreement.

6. *Given the illegal invasion of Ukraine by Russia and the involvement of Belarus, there is currently no appropriate context allowing the implementation of the actions foreseen in this programme with legal entities established in Russia, Belarus, or* in non-government controlled territories of Ukraine. Therefore, such legal entities are not eligible to participate in any capacity. Exceptions may be granted on a case-by-case basis for justified reasons. This criterion also applies in cases where the action involves financial support given by grant beneficiaries to third parties established in Russia, Belarus or in non-government controlled territories of Ukraine (in accordance with Article 204 of the Financial Regulation No 2018/1046).

3. TECHNICAL DESCRIPTION OF THE TOPICS FOR THE CPL

3.1 Chips-CPL-1 Pilot line on advanced sub 2nm leading-edge system on chip technology

Chips-CPL-1	
Max EU Expenditure • Joint procurement • Setup, integration HORIZON-Chips-2023-IA-CPL-1 • Operational DIGITAL-Chips-2023-SG-CPL-1	Max. EURO 700 Mio Indicative EURO 200 Mio; Max EURO 240 Mio Indicative EURO 460 Mio; Max EURO 550 Mio Indicative EURO 40 Mio; Max EURO 40 Mio
Mode	Call for Pilot Line (CPL)
Publication date	1 December 2023
Deadline Submission of proposals	29 February 2024 at 17:00 Brussels Time

Context

Microelectronics is a key technology and industry that underpins the value and supply chains of almost all business models today, in particular in the light of the current digital aspirations of global economies and societies. Thus, European competitiveness in leading-edge semiconductor technologies is essential to meet the evolving performance and efficiency demands of these widespread digital applications.

The access to an advanced 300mm R&D pilot line for advanced leading-edge (sub-2nm) system on chip technology will significantly strengthen the European semiconductor ecosystem. This system on chip pilot line will deliver the essential building blocks for the advanced semiconductor roadmap and will demonstrate novel device architectures using advanced technology modules ‘at pitch’. It will provide technology options elaborated with a strategy and operational focus towards leading-edge semiconductor manufacturing. Besides validating the emerging device architectures and interconnect options, it synchronizes with the industry timeline of the most advanced applications. Given that advanced system design and technology will require close interaction, such early insight will boost the European design and application ecosystem for the most advanced nodes. This will allow to leverage the most advanced technology modules (lithography, advanced logic, memory, advanced interconnect, etc.).

In this context, it is **proposed that Europe shall be equipped with a pilot line that will develop the required building blocks to further advance the sub 2nm system on chip technology** and that will enable companies and academia to design, process and validate their component, system and application ideas based on the most advanced technology options. It shall encompass the set-up of a leading-edge 300mm platform based on cutting edge equipment with advanced semiconductor processes and fabrication technologies. This pilot line should aim to significantly accelerate industrialization and time-to-market resulting in a competitive advantage for the European semiconductor ecosystem.

Expected outcomes

The proposed pilot line shall be established with all the necessary equipment, facilities, and target the following main **objectives**:

- **Next generation sub 2nm technology** with all the functionalities, for an innovative offering to **European academic and industrial semiconductor partners, strengthening the European industry innovation capacity and** opening new opportunities for future market leadership.
- **Process modules** for enhancing the functionalities of the sub 2nm technology including advanced logic modules, advanced non-volatile embedded memories and advanced interconnects at die and wafer level . The validated technology modules and device integration flows will provide early models and research Process Design Kits to enable design and system level exploration and demonstration.
- **Demonstration of the baseline flows** to validate the options for the advanced sub 2nm SoC technology and to enable to explore and quantify its performance consumption for new applications in areas like computing, 5G/6G, automotive etc. in a full-stack innovation approach through access to the Pilot Line
- **Deliver validation** of new process modules **for future equipment and materials**, to strengthen European leadership in critical processing steps, such as leading-edge lithography, deposition, etching, wafer processing, packaging, process metrology, automation.
- **A sustainable pilot line open to European stakeholders (**especially for SMEs and start-ups) across the whole value chain, from materials to applications and thereby creating a **community of interest for those technologies, boosting the use of those technologies in Europe**. The pilot line should significantly boost the innovation capacity on advanced semiconductor systems resulting in a competitive advantage for the European ecosystem.

The **expected results** for this pilot line should therefore comprise:

- Offering to Europe a domestic semiconductor R&D demonstration and exploration option for advanced sub 2nm SoC technologies.
- Promoting the exploration of the key benefits of these technologies and giving to Europe the opportunity to have early access to the miniaturization evolution of electronics on a wide spectrum of semiconductors markets such as heterogeneous advanced computing paradigms, Automotive, Space, Manufacturing 4.0, IoT and Edge AI domain.

- Expanding the sub 2nm SoC European technology platform ensuring:
    - **Exploring all options in the scaling roadmap to prepare for the 'Angstrom' nodes.**
    - **Strengthening of the European leadership in equipment and materials** thanks to a world-wide unique facility for demonstration and integration of new process modules**.**
    - **Generating intellectual property** at various levels.
    - **Memories and Advanced interconnect modules**: to enrich the platform with non-volatile memories and novel high-density interconnects to enable a broad spectrum of advanced SOC options
    - **IC Design ecosystem:** to strengthen the design ecosystem and value chain around sub 2nm SoC technology options thanks to design platforms and competences centers, skills and expertise.
    - **Delivering (research) PDKs and making them available to third parties allowing them to** explore and model new IC architectures as well as numerous IPs on advanced applications taking advantages of the advanced SoC options and chiplet technology evolutions that allow combining various functionalities.
- Expanding the European user base of this technology and build a community of interest around this technology.
- Access to those advanced technologies, specifically by SMEs and Start-ups with the support of the Competence Centers to be started by the Chips JU.
- Early research Process Design Kits for the design platform and support to the design platform for those kits.
- A collaboration with the other pilot lines established under the Chips JU, creating a strong networked European environment for advanced chip technologies.

Scope

The proposed pilot line needs to work at all levels of the main technological steps:

- **Development of the sub 2nm technology modules for enhancing the performance of the current technology**, through reshaping the transistor architecture and introduction of disruptive materials and process technology options. . The main technologies to be developed need to be **aligned with the advanced technology requirements expressed in international research roadmap(s) at device (logic, memory) and interconnect level.**. They should be performed through a strong interaction between the process and design teams in order to optimize the sub 2nm SoC performance, and to deliver the research PDKs for each developed technology and process modules to that effect.

- **Development of the crucial SoC-enabling process modules:**
    - *Memories*: The Pilot Line should include advanced NVM in the metal interconnections. These can offer new ranges of applications and would allow breakthroughs in new

paradigms for computing. Novel emerging memory options should be explored to be validated by the pilot line users in collaboration with other pilot lines.

- *System On Chip options*: The Pilot Line should offer design and architecture options compatible with new 3D architectures, chip-on-wafer and wafer-to-wafer alignment technologies and efficient bonding techniques as well as high density advanced interconnects such as nano TSV's to enable the 3D SoC at the die level and continue the performance increase and cost reduction enabled by sequential 3D monolithic integration for specific applications.

- **Delivery of modules at pitch for next generation equipment and materials.** R&D for such complex process technology should entail collaborative activities with equipment and material suppliers on base step, sub-module and module level innovations and mutual impact assessment of process steps in a flow. A substantial amount of characterization and fundamental studies of materials properties and interfaces is also required.
- **Delivery of updated research PDKs**

  Once the technology and additional process module are mature enough the proposed pilot line should continuously deliver updated (research) PDKs of the developed technologies for technology assessment.

  Any stakeholder must have access to these PDKs, and the additional modules through the Design Platforms, the Competence Centers and/or directly to the Pilot Line.

- **Realization of early research demonstrations and (virtual) system exploration through MPW runs for European partners,** according to an operational and access policy defined for the pilot line for the collaboration with those stakeholders.

  The access policy from the different stakeholders to the pilot line should be defined in the proposal according to fair and non-discriminatory principles.

  During the whole duration of the pilot line, the hosting entity and other partners should provide training to any European partner interested in designing devices based on the pilot line technology in order to use the full benefits of this technology, as well as for students for up- and re-skilling in order to attract new talents in the European semiconductor industry.

  Collaborations: The proposed pilot line must facilitate the collaboration with other pilot lines, with design platforms and competence centers to allow contributions from other stakeholders that develop a strong expertise in a specific domain related to the topics of this pilot line.

3.2 Chips-CPL-2: Pilot line on advanced Fully Depleted Silicon On Insulator technologies targeting 7nm

Chips-CPL-2	
Max EU Expenditure • Joint procurement • Setup, integration HORIZON-Chips-2023-IA-CPL-2 • Operational DIGITAL-Chips-2023-SG-CPL-2	Max. EURO 420 Mio Indicative EURO 200 Mio; Max EURO 200 Mio Indicative EURO 210 Mio; Max EURO 330 Mio Indicative EURO 10 Mio; Max EURO 10 Mio
Mode	Call for Pilot Line (CPL)
Publication date	1 December 2023
Deadline Submission of proposals	29 February 2024 at 17:00 Brussels Time

Context

The 2D Fully-Depleted Silicon on Insulator (FD-SOI) transistor architecture offers a distinct advantage over 3D transistors competing technologies, especially for the Ultra-Low Power logic and analog/mixed signal applications. FD-SOI enables a high range of Body Bias, which allows to adjust dynamically the High Performance (HP) / Low Power (LP) trade-off either of a running circuit or a portion of circuit. This unique capability allows switching from LP to HP mode only when necessary and minimizes the overall power consumption, which is a major factor to enable a continuous integration of new functions in circuits, and to achieve an optimum power efficiency.

The strong increase of demand for FD-SOI chips explains the investments of European stakeholders to increase their manufacturing capacity to produce 22nm and 18nm FD-SOI chips in Europe. To highlight how significant is the expected increase of the FD-SOI chips, analysts predicted that the SOI wafer market would double from 2021 to 2026 to reach $ 2.3 billion by 2026, at a CAGR of 17.2%[1].

For the current 28 and 22nm FD-SOI customers, the availability in Europe of a 10-7nm FD-SOI node is of paramount importance for their products evolution and competitiveness

[1] Silicon on Insulator (SOI) Market with COVID-19 Impact Analysis by Wafer Size (200 mm and less than 200 mm, 300 mm), Wafer Type (RF-SOI, FD-SOI), Technology (Smart Cut), Product, Application (Consumer Electronics, Automotive) - Global Forecast to 2026- https://www.researchandmarkets.com/reports/5129002/silicon-on-insulator-soi-market-with-covid-19

compared to the more advanced FinFET nodes while keeping a strong benefit for analog, mixed signals and RF applications.

The European customers involved in the development of automotive and edge-AI processors, smart sensors and imagers, 5G/6G, RF connectivity, wearable and medical devices, IoT, and cybersecurity devices, will be interested in getting access to a European FD-SOI supply chain that provides an excellent Speed/Power/Cost trade-off at advanced technology nodes. This trade-off, which should be available in this pilot line, is key for the market strengths and sovereignty of Europe.

FD-SOI is a very promising technology to meet the demands for the European AI, and 6G agendas but it also strengthens Europe in the fields of More-than-Moore markets, quantum computing on silicon, cryoCMOS electronics, trusted chips and components for Space applications.

In this context, it is **proposed that Europe should be equipped with a pilot line that will develop the required building blocks to further advance the FD-SOI towards 7 nm technology**.

Expected outcomes

The proposed pilot line shall be established with all the necessary equipment, facilities, and shall target the following main **objectives**:

- **Next FD-SOI generation 10nm and 7nm technology** with all the functionalities (new substrates, Front-End-Of-Line, Middle-of-Line and Back-End-Of-Line), and its adaptation to a wide range of More-than-Moore (MtM) applications, for a transfer of technology to European semiconductor partners, strengthening the European industry manufacturing capacity and opening new market opportunities.
- **Process modules** for enhancing the functionalities of the FD-SOI 10-7nm technology including advanced embedded non-volatile memories (NVM) : MRAM, OxRAM, PCRAM, FeRAM…, the investigation of its compliance with 3D options such as 3D assembly, 3D heterogeneous integration technology and Monolithic 3D offering new capabilities for integrated photonics, RF components capabilities and introduction of III-V materials.
- **Demonstrators** to validate the achievement of the advanced FD-SOI technology and to quantify its performance and low energy consumption for various applications, such as RF and optical communications, IoT, image sensors, cybersecurity, displays, AI.
- **A sustainable pilot line open to all European stakeholders (**especially SMEs and startups) from the whole value chain, from materials to applications, and thereby creating a **community of interest for those technologies, boosting the use of those technologies in Europe**.

The **expected results** for this pilot line should therefore comprise:

- **Offering to Europe a domestic semiconductor prototyping option for advanced FD-SOI technologies with smart combinations of embedded non-volatile memories and 3D options** allowing a path to disruptive Integrated Circuit Architectures and to contribute to the twin Green and Digital transitions.
- **Promoting FD-SOI technology and giving to Europe the opportunity to follow the miniaturization evolution of electronics on a wide spectrum of semiconductors markets** such as MtM, Automotive, Space, Manufacturing 4.0, IoT and Edge AI domain.

- **Expanding the FD-SOI European technology platform ensuring**:

- **Downscaling technology**: to prepare the 10-7nm FD-SOI technology and devices.
- **Generating intellectual property** at various levels.
- **Memories and 3D options**: to enrich the FD-SOI platform with non-volatile memories (PCRAM, OxRAM, FeRAM and MRAM) and 3D options (monolithic 3D and 3D stacking)
- **IC Design ecosystem:** to strengthen the FD-SOI design ecosystem and value chain around FD-SOI manufacturing thanks to design platforms and competences centers, skills and expertise.
- **Allowing stakeholders third parties thanks to PDK delivery to build the future** by developing new IC architectures as well as numerous IPs on advanced applications taking advantages of the FD-SOI for mixed circuits.
  - Expanding the European user base of this technology and build a community of interest around this technology.
  - Access to those advanced technologies, specifically by SMEs and Startups with the support of the competence centers to be started by the Chips JU.
  - Process Design kits for the design platforms and support the design platforms for those kits.
  - A collaboration with the other pilot lines creating a strong networked European environment for advanced chip technologies.

Scope

The proposed pilot line shall work at all levels of the main technological steps:

- **Development of the 10nm to 7nm FD-SOI technology modules for enhancing the performances of the current FD-SOI technology**, including RF applications, through reducing the transistor size. The main technologies to be developed shall be: the enhancement of the carrier mobility, the optimization of the transistor process, the development of the Middle-of-Line (MoL) modules and the development of Back-End-of-Line (BEOL) process modules. They should be performed through a strong interaction between the process and design teams in order to optimize the FD-SOI device performances, and to deliver the PDKs for each developed technology and process modules.

- **Development of the additional process modules.**
  - ***Memories***: The Pilot Line platform should be enhanced by adding in the metal interconnections. These additions can offer new ranges of applications and would allow breakthroughs like in-memory computing. Several memory NVM options (PCRAM,

FeRAM, OxRAM, MRAM etc.) will have to be proposed to the pilot line partners, by themselves or in collaboration with other pilot lines.

- ***3D options***: The Pilot Line should offer design environments compatible with new 3D architectures, chip-on-wafer and wafer-to-wafer alignment technologies and efficient bonding techniques. 3D option based on monolithic sequential integration should also be proposed to further improved performances and decreased cost.

- **Delivery of updated PDKs**
  - Once the technology and additional process module will be mature enough, the proposed pilot line will have to continuously deliver updated PDKs of the developed technologies for technology assessment.
  - Any stakeholder must have access to the PDKs, describing the updated 10-7nm FD-SOI technology and the additional modules through the Design Platforms, the Competence Centers and/or directly to the pilot line.
- **Realization of circuits through Multi-Project-Wafers (MPW) runs for European partners,** according to an operational and access policy defined for the pilot line for the collaboration with those stakeholders.

  The access policy from the different stakeholders to the pilot line should be defined in the proposal according to fair and non-discriminatory principles.

  During the whole duration of the pilot line, the hosting entity and other partners should provide training to any European partner interested in designing devices based on FD-SOI technology in order to use the full benefits of this technology, as well as for students for up- and re-skilling in order to attract new talents in the European semiconductor industry.

  Collaborations: The proposed FD-SOI pilot line must facilitate the collaboration with other pilot lines, with design platforms and competence centres to allow contributions from other stakeholders that develop a strong expertise in a specific domain related to the topics of this pilot line.

3.3 Chips-CPL-3: Pilot line on advanced Packaging and Heterogenous Integration

Chips-2023-CPL-3	
Max EU Expenditure • Joint procurement • Setup, integration HORIZON-Chips-2023-IA-CPL-3 • Operational DIGITAL-Chips-2023-SG-CPL-3	Max. EURO 370 Mio Indicative EURO 200 Mio; Max EURO 260 Mio Indicative EURO 149 Mio; Max EURO 210 Mio Indicative EURO 21 Mio; Max EURO 30 Mio
Mode	Call for Pilot Line (CPL)
Publication date	1 December 2023
Deadline Submission of proposals	29 February 2024 at 17:00 Brussels Time

Context

The continuous demand for higher functional diversity, along with the slowdown of Moore's law, has induced in recent years a disaggregation of the chip design to better exploit the different existing capabilities of whatever process node or technology that deliver the best functionalities. Those chiplets are reaggregated at package level leading to systems in package. These new concepts of heterogeneous integration enable going well beyond monolithic processes and are becoming more prominent at a fast pace, while enabling keeping the cost of those integrated systems affordable.

This trend also sees functionalities usually available at the circuit board level being moved upstream added closer to the chip level through the packaging technologies, e.g. through interposers or 3D-chip-on-chip concepts.

But creating such designs today, where multiple custom chips or chiplets are being integrated, is equivalent of doing multiple custom designs, which is expensive. Heterogeneous integration and advanced packaging are therefore essential to enable those functionalities, reduce energy consumption and fabrication yield loss of integrated systems and mitigate the related costs. This trend must therefore be accompanied by adequate design tools, manufacturing strategies as well as advanced test methodologies.

Efforts will also need to be dedicated to standardizing design methodologies, test and technologies to reduce custom developments while addressing a wide range of application sectors, e.g. computing, automotive, communications, etc.

In this context, it is **proposed that Europe should be equipped with a pilot line to develop the necessary building blocks from design, through processes, assembly to advanced testing of a wide range of heterogeneous integration technologies**.

Expected outcomes

The proposed pilot line shall be established with all the necessary equipment, facilities, and target the following main **objectives**:

- **Next generation technologies for advanced packaging and heterogeneous integrated systems** combining chips and chiplets from different domains: logic, memory, sensing, photonics, RF and communication, for a transfer of technology to European semiconductor partners, strengthening the European industry manufacturing capacity and opening new market opportunities.
- **Advanced packaging concepts**, for edge computing, AI, quantum technologies and communication in small form factors.
- **New process modules** ensuring quality, reliability and security of hetero-integrated chips and systems.
- **Design methodologies** for heterogenous integrated systems into a single package with improved performances like cost effectiveness, improved energy efficiency, reduced ecological footprint, high reliability etc..
- **Demonstrators** to validate the achievements of the developed technologies covering the different domains of application.
- **A sustainable pilot line open to European stakeholders (**especially for SMEs and start ups) from the whole value chain, from materials to applications, and thereby creating a **community of interest for those technologies, boosting the use of those technologies in Europe**.

The **expected results** for this pilot line should therefore comprise:

- Offering to Europe a domestic prototyping option for advanced packaging and heterogenous integration.
- Promoting advanced packaging and heterogenous integration technology and giving to Europe the opportunity to apply it:
  - For advanced communications, enabling a European ecosystem that can support heterogeneous integration to capture higher value in the connectivity market. This is also essential to fulfilling the transition towards the Green Deal objectives through control and forecasting systems.
  - For mobility, enabling autonomous driving, the developed technologies shall provide ways to design and manufacture new environmental sensors, which e.g. simplify and improve object and lane detection, work in difficult weather conditions and situations.
  - For advanced IoT and Edge-AI concepts with minimal form factor, low power consumption and low cost
- Expanding the European technology platform ensuring:
  - Advanced technology.
  - Generating intellectual property.
  - Design kits and tools to enable this technology and making it accessible to a larger.

- Expanding the European user base of this technology and build a community of interest around this technology.
- Access to those advanced technologies, specifically by SMEs and Start Ups with the support of the competence centers to be started by the Chips JU.
- Process Design kits for the design platform and support the design platform for those kits.
- A collaboration with the other pilot lines creating a strong networked European environment for advanced chip technologies.

Scope

The pilot line shall provide a platform for chiplet integration.

- This platform shall enable 2.5D and 3D heterogeneous integration for multiple core technologies (CMOS, Opto/RF) and devices (MEMS, Opto). It should enable chiplet integration of advanced nodes from external sources. As an important technology basis, fan-out and fan-in wafer level packaging should be developed for the different integration concepts. In the same way, through-x via and interposer technologies should be developed for the materials of interest. Those include silicon, glass, silicon carbide, polymers. Besides the latter materials, III-V materials should be part of the mix to enable interfaces with RF and photonics functions. And to enable a varied integration mix, diverse bonding technologies should be developed as building blocks as relevant, e.g. micro-solder-bump bonding, wafer-wafer-bonding, die-to-wafer-bonding and hybrid Cu-Cu bonding for extreme pad-pitches below 0.5 µm.
- The packaging technologies shall address the 200mm and 300mm wafer platforms since both are relevant for modern components. Where relevant, it is expected that the pilot line provides capacity for large scale organic interposer technology as panel integration as well.
- The developed technologies shall provide interfacing capability to semiconductor device integration. This means that different interface concepts and technologies should be developed for:
- RF and in particular millimetre-wave and beyond
- Advanced photonic functionalities, including integrated photonics
- Direct integration of sensors and MEMS solving the specific constraints of mechanical and thermal stresses
- Integration of novel energy-efficient non-volatile memory technologies
- Integration of novel functionalities with power electronic components
- System design is becoming an inherent component of advanced packaging. System technology co-optimization methodologies and tools should be developed through the pilot line to ensure they serve a holistic implementation of chiplet architectures through the system development flow (chiplet to system) where the package is an integral part of the system functionality. This comprehensive end-to-end design flow and methodology for chiplet-based advanced heterogeneous system integration will implement the Design-for-Testability, -Manufacturing, -Reliability, -Security methodologies as and where relevant. Those are essential enablers to ensure that the developed design and process flows are transferable to industrial environments and will be made available to a large community in cooperation with the design platform.

- Characterization, test and reliability are becoming increasingly complex when integrating multiple functional chiplets in a single package. Therefore, novel test concepts and technologies for function-, quality- and yield- optimization should be developed. This must inter alia cover non-destructive 3D imaging and defect metrology, improved electrical fault isolation, high-throughput destructive characterisation to isolate and study defects.
- This should be complemented by methods to fight against counterfeits, a growing concern while moving to chiplet-based systems.
- To increase the reliability of systems in the field, built-in self-test methodologies and functionalities should be proposed, and their integration developed.

The access policy from the different stakeholders to the pilot line should be defined in the proposal according to fair and non-discriminatory principles.

During the whole duration of the pilot line, the hosting entity and other partners should provide training to any European partner interested in designing devices based on the pilot line technology in order to use the full benefits of this technology, as well as for students for up- and re-skilling in order to attract new talents in the European semiconductor industry.

Collaborations: The proposed pilot line must facilitate the collaboration with other pilot lines, with design platforms and competence centres to allow contributions from other stakeholders that develop a strong expertise in a specific domain related to the topics of this pilot line.

3.4 Chips-CPL-4: Pilot line on advanced semiconductor devices based on Wide Bandgap materials

Chips-CPL-4	
Max EU Expenditure • Joint procurement • Setup, integration HORIZON-Chips-2023-IA-CPL-4 • Operational DIGITAL-Chips-2023-SG-CPL-4	Max. EURO 180 Mio Indicative EURO 100 Mio; Max EURO 140 Mio Indicative EURO 70 Mio; Max EURO 70 Mio Indicative EURO 10 Mio; Max EURO 10 Mio
Mode	Call for Pilot Line (CPL)
Publication date	1 December 2023
Deadline Submission of proposals	29 February 2024 at 17:00 Brussels Time

Context

The twin digital and energy transitions have increased the demand for, and the potential market of electronic devices across a range of applications, from electric vehicles (EVs) to 5G/6G communication systems. In these domains, however, traditional silicon–based semiconductor devices present inherent constraints in achieving the efficiency, speed, and power handling capabilities increasingly demanded by evolving industries and technological advancements. This has led to a growing focus, at the industrial and research level, on wide bandgap (WBG) semiconductors, particularly silicon carbide (SiC) and gallium nitride (GaN), driven by their superior electrical properties, including higher power efficiency, high–temperature operation, and faster switching speeds. These characteristics make WBG materials essential in various industrial and economic activities driven by the development of highly efficient power and radio frequency (RF) electronics. These include the increasing emphasis on energy efficiency, the integration of renewable energy, the electrification of transportation, the overall advancement in the operation and control of electric motors used in various industrial processes, the expanding need for wireless communication, the evolution of communication standards, the growth of IoT and connected devices, advancements in 5G technology, and the integration of power and RF technology into various industries and applications.

The European semiconductor industry competes very effectively in this section of the microelectronics industry, but in recent years WBG semiconductors have seen a raise in investment across Europe's competitors, with governments and corporates investing significant resources to develop the next generation of WBG-based devices. The current challenge for players in this field is to (i) improve the yield and reduce the cost of producing devices with current WBG technologies and (ii) develop new devices and applications based on SiC and GaN as well as a wider group of WBG and ultra–WBG (UWBG) semiconductors.

As a result, it is crucial for Europe to:

- Maintain its technological leadership in GaN and SiC, extending it to UWBG materials.
- Strengthen Europe's supply chain capacities, especially with respect to WBG and UWBG semiconductor production and development.
- Develop the next generation of highly efficient power and RF devices to foster the twin digital and energy transitions.

Expected outcomes

The call will contribute to further expand the competitiveness of the European semiconductors industry and to improve the efficiency of the hi–end portion of the advanced power device portfolio and the related value chain based in Europe. It will focus on two key outcomes: *(i)* to extend the maturity level and the impact of SiC and GaN technologies; and *(ii)* to explore less

mature WBG and UWBG semiconductors, such as cubic polytype of SiC (3C–SiC), low–cost polycrystalline SiC, lattice–matched InAlN or InAlGaN for RF heterostructures, bulk gallium nitride or gallium oxide (Ga_2O_3) or aluminium nitride (AlN).

Proposal results are expected to contribute to:

- developing advanced processes and equipment for WBG and UWBG semiconductors with applications in power, high–frequency and RF electronics;
- cost optimization and yield improvement for WBG processing;
- developing and demonstrating process flow, with a high level of automation, yield, and throughput, compatible with industrial manufacturing standards;
- developing enabling process and integration techniques for devices in a cost–effective manufacturing environment;
- designing and manufacturing application–driven device demonstrators to validate their manufacturing readiness level and establish their commercial value and potential for targeted markets.
- access to advanced WBG technologies by industry including SMEs and Startups with the support of the competence centers to be established by the Chips JU.
- development of comprehensive and well-documented Process Design Kits (PDKs) specific to the WBG technologies and their maturity, offered by the pilot line;
- support for the Design Platform on the PDK specifically developed for WBG technologies;
- allow third parties to invest in their future by developing new IC architectures and Ips on advanced applications taking advantages of WBG devices and circuits and thanks to PDK delivery

Scope

The pilot line should address most of the following topics:

- Further optimization and development of WBG and UWBG substrates and advanced growth techniques, and in particular:
    - SiC including off-axis and different polytypes
    - GaN crystal growth and substrates (e.g. n-types and semi-insulating)
    - UWBG native substrates (e.g., AlN, Ga_2O_3)
- Extending the current state–of–the–art device technology on wafers and epi–wafers:
    - SiC epi materials on 200mm and alternative low–cost SiC wafer solutions
    - III–Nitrides on off–axis SiC and 3C–SiC
    - GaN on Si, GaN–on–GaN, Ga_2O_3
    - introduction of novel high–k dielectrics for the next generation of 4H–SiC MOSFETs and CMOS
    - III–Nitrides HEMT epi on SiC

- Further work on device processing and reliability, including:
    - optimization of SiC MOSFET in a wide power range
    - RF HEMTs, power HEMTs, GaN process modules
    - Vertical FinFETs
    - GaN MISHEMTs, vertical GaN
    - Novel architectures for SiC MOSFET and BJT
    - Gate insulators trapping, identification of critical defects and qualification of substrates
- Further development of WBG–based advanced devices and ICs:
    - Large–scale integration
    - development of integrated circuit SiC–based technology for harsh environments and radiation hard operations
    - development of advanced normally–off RF GaN HEMTs
    - MMIC design kits and processes
    - Power IC design
- Delivery of updated PDKs: Once the technology and additional process modules will be mature enough, the proposed pilot line will have to continuously deliver updated PDKs for technology assessment. Any stakeholder must have access to the PDKs, describing WBG technology and the additional modules, through the Design Platforms, the Competence Centers and/or directly to the pilot line.
- Realization of Power and RF devices through dedicated runs for European partners, according to an operational and access policy defined for the pilot line for the collaboration with those stakeholders.

  The access policy from the different stakeholders to the pilot line should be defined in the proposal according to fair and non-discriminatory principles.

  During the whole duration of the pilot line, the hosting entity and other partners should provide training to any European partner interested in designing devices based on WBG technology to use the full benefits of this technology, as well as for students for up- and re-skilling to attract new talents in the European semiconductor industry.

  Collaborations: The proposed WBG pilot line must facilitate the collaboration with other pilot lines, with design platforms and competence centres to allow contributions from other stakeholders that develop a strong expertise in a specific domain related to the topics of this pilot line.

4 DESCRIPTION OF THE CALL FOR PILOT LINES (CPL)

Proposals for the pilot lines will be collected through a Call for Pilot Line (CPL).

The document describing the CPL and every facet of this call including the necessary elements for the 3 interrelated calls is included in this chapter and will be used to launch the calls as it contains the details of the procedure.

To launch the calls each pilot line call will merge the technical description of the topic and specific budgets given in chapter 3 with the Call Document in this chapter. The Annexes mentioned in this chapter are collected at the end of this chapter.

Call text

Chips Joint Undertaking

REF: Chips-CPL-XX

CALL FOR [pilot line]

1 INTRODUCTION – CONTEXT AND BACKGROUND

1.1 Legal framework

The Chips Joint Undertaking (hereinafter "Chips JU") is established by Council Regulation (EU) 2021/2085 establishing the Joint Undertakings under Horizon Europe[2] (hereinafter "SBA") and modified by an amendment, Council Regulation (EU) 2023/1782 of 25 July 2023[3].

The Chips for Europe Initiative is established under Regulation (EU) 2023/1781 of 13 September 2023[4] (hereinafter "Chips Act"). One objective of the Chips Act is to ensure the conditions necessary for the competitiveness and innovation capacity of the Union. In this context, the Chips for Europe Initiative (the 'Initiative') established by the Chips Act aims to support this objective by bridging the gap between the Union's advanced research and innovation capabilities and their sustainable industrial exploitation.

The Initiative shall promote capacity building to enable design, production and systems integration in next-generation semiconductor technologies, and should enhance collaboration among key players across the Union, strengthening the Union's semiconductor supply and value chains, serving key industrial sectors and creating new markets.

Pilot lines are one of the components of the Initiative. Concretely, the Initiative will support the enhancement of existing and development of new advanced pilot lines to enable development and deployment of cutting-edge semiconductor technologies and next-generation semiconductor technologies. These pilot lines shall provide for the industry a facility to test, experiment and validate semiconductor technologies and system design concepts.

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2 OJ L 427, 30.11.2021, p. 17–119.
3 OJ L 229, 18.9.2023, p. 55–62.
4 OJ L 229, 18.9.2023, p. 1–53

The above is further defined in Article 3 ("Establishment of the Initiative"), Article 4 ("Objectives of the Initiative") and Article 5 ("Content of the Initiative") of the Chips Act. Article 4(2)(b) makes reference to "operational objective 2" which mentions "*enhancing existing and developing new advanced pilot lines across the Union to enable development and deployment of cutting-edge semiconductor technologies and next-generation semiconductor technologies*". Article 5(b) further specifies the content of this operational objective on pilot lines, namely that "*the Initiative shall, under its operational objective 2*:

(i) *strengthen capabilities in next-generation chip production technologies and manufacturing equipment, by integrating research and innovation activities and preparing the development of future technology nodes, such as leading-edge nodes, fully depleted silicon on insulator technologies, new semiconductors materials or heterogeneous systems integration and advanced module assembly and packaging for high, medium or low volumes;*

(ii) *support innovation at a large scale through access to new or existing pilot lines for experimentation, test, process control, final device reliability and validation of new design concepts integrating key functionalities;*

(iii) *provide support to integrated production facilities and open EU foundries through preferential access to the new pilot lines, as well as ensure access on fair terms to new pilot lines for a wide range of users of the Union's semiconductor ecosystem".*

Article 12(1) of the Chips Act entrusts the implementation of the Initiative's operational objectives 1-4 to the Chips JU. Therefore, operational objective 2 on pilot lines will be implemented by the Chips JU.

1.2 Budget

The Chips JU proceeds to the implementation of pilot lines which will be co-financed by the Union and the participating states. The Chips JU shall be tasked with providing financial support, through any instrument or procedure provided for in Horizon Europe[5] (hereinafter "HE") and the Digital Europe Programme[6] (hereinafter "DEP").

In accordance with recital (6) of the SBA Amendment, throughout the lifetime of the Chips Joint Undertaking, up to EUR 2,875 billion shall be dedicated to the Initiative. Of that amount, EUR 1,450 billion shall be for capacity-building activities for operational objectives 1 to 4 and EUR 1,425 billion shall be for research and innovation activities related to operational objectives 1 to 4.

[5] Regulation (EU) 2021/695 of 28 April 2021 establishing Horizon Europe – the Framework Programme for Research and Innovation, laying down its rules for participation and dissemination, and repealing Regulations (EU) No 1290/2013 and (EU) No 1291/2013

[6] Regulation (EU) 2021/694 of 29 April 2021 establishing the Digital Europe Programme and repealing Decision (EU) 2015/2240

Furthermore, Article 128(4) of the SBA Amendment indicates that the Union's contribution from DEP may not exceed 50% of the total costs of capacity-building activities.

It must be noted as well that, in accordance with Article 129(4) of the SBA Amendment, the participating states are allowed to report financial contributions made since 8 February 2022 (date of publication of the Chips Act package) if the conditions set out in Article 129(4) SBA are fulfilled. In their applications, applicants need to specify what costs would be within the scope of this Article.

1.3 The overall implementation process

Implementing an advanced pilot line is a complex endeavour requiring a coordinated effort of multiple procurements of equipment and tools, as well as set-up and integration activities related to those equipment and tools to achieve a specific technologically advanced infrastructure that then can be used by industry, both large enterprises, SMEs and startups, as well as academia.

Given the important role that a pilot line has in bridging the gap between the Union's advanced research and innovation capabilities and their sustainable industrial exploitation, the Chips Joint Undertaking should co-own 50% of the tools and equipment that constitute a pilot line as permitted by Article 3(4) of the SBA and Article 43(5) of the Financial Rules of the Chips JU [7]. This will allow the Chips Joint Undertaking to keep a closer control over such strategic infrastructures, thereby making future reporting exercises towards auditing authorities more transparent and straightforward.

1.3.1 The Hosting Consortium

A consortium needs to include:

a) at least one independent legal entity established in a Member State; and
b) at least two other independent legal entities each established in different Participating States[8].

Furthermore, the consortium (hereinafter 'Hosting Consortium'), will be composed of one or more Hosting Entities (i.e., entities that are hosting part or all of the equipment and tools of the pilot line – see further below) and possibly other members (members of the consortium that do not host any tools and equipment of the pilot line). One of the consortium members acts as the coordinator; typically, but not necessarily, the coordinator is a Hosting Entity. The coordinator will be mandated by the Hosting Consortium to act on behalf of the other members of the consortium (e.g., to sign the Hosting Agreement – see Annex 2).

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7 Chips GB decision 2021.02 (Annex 12) approving the Financial Rules, re-adopting the previously adopted decision ECSEL GB 2020.138 (see link)

8 It must be noted that entities established in Participating States that are associated countries (i.e., not in a Member State) will only receive funding from the Programme (HE and/or DEP) their countries are associated to.

The pilot line can be physically located at one or several hosting sites. A hosting site is the physical facility at which a Hosting Entity will host and operate a pilot line and which is established in a Participating State that is a Member State. It must be noted that a pilot line may be distributed across different hosting sites that are located in different Member States.

A consortium including Hosting Entity(ies) will be selected for setting up and running a pilot line. The consortium will have as **main responsibilities**:

- to manage joint procurements, if certain conditions are fulfilled (see under Section 1.3.3.1): this requires having the necessary expertise and the staff to execute joint procurements;
- to install, commission and host the procured equipment and tools on the hosting site(s). Therefore, all hosting sites need to have the proper infrastructure (so-called cleanrooms and other technical facilities) and the proper staff;
- to execute (for pilot lines that are located on different sites, in a coordinated way) the different activities that will lead to a technologically advanced pilot line and to offer all its services (such as access by third parties, etc.) ultimately realising the objectives of the pilot line.

1.3.2 The present Call Document

Taking into account the abovementioned responsibilities of a Hosting Consortium, the present Call Document includes three interrelated calls:

- A **Call for Expression of Interest** (hereinafter "CfEoI") for the selection of a Hosting Consortium. Provided certain conditions are fulfilled by the Hosting Entity(ies) of the Hosting Consortium (see Section 1.3.3.1 below), this CfEoI will entitle the selected Hosting Entity(ies) to manage the procurement of the tools and equipment of the pilot line to be acquired under a joint procurement agreement (JPA – enclosed as Annex 3).
- A **Call for proposals for the Set-up, integration and process development** grant funded under the Horizon Europe Programme. The type of action is a Research and Innovation Action (RIA).
- A **Call for proposals for the operational activities** of the pilot line, funded under the Digital Europe Programme. The type of action is a Simple Grant.

In practice, this means that an applicant consortium will have to submit one application that will include three interrelated proposals, one for each of the abovementioned calls. Each call will have its specific evaluation criteria, as outlined in Section 5 of the present Call Document. A consortium will only be eligible for funding if its proposal for all three calls passes the necessary thresholds.

All three calls will close on the same date.

Together with the present Call Document, the following documents[9] are published:

Annex 1	Application form template
Annex 2	Draft Model Hosting Agreement
Annex 3	Draft Model Joint Procurement Agreement
Annex 4	Model Letter of Intent describing the formal commitment of each Participating State (PS) to financially support the pilot line and its participating Consortium members
Annex 5	HE model grant agreement for the R&D activities of the pilot line
Annex 6	DEP model grant agreement for the operational activities of the pilot line

In addition to the above documents which are annexed to the present Call Document, additional documents will be published that are relevant in case of State aid notification. These documents should not be submitted to any of the three calls above. These documents are:

- Funding gap template;
- Notification template, which indicates the information a Member State needs to provide (see Section 1.3.5).

1.3.3 Submission of an application to the present Call Document

Applicants may submit applications to the present Call Document by filling in the ***application form (Annex 1 to the present Call Document)***. The application should serve as:

- An expression of interest to be submitted to the Call for Expression of Interest for the selection of a Hosting Consortium for the pilot line;
- A proposal to be submitted to the Call for Proposals for Set-up, integration and process development (Horizon Europe, Research and Innovation Action);
- A proposal to be submitted to the Call for Proposals for Operational activities of the pilot line (Digital Europe Programme, Simple Grant).

[9] Some of these documents are drafts. After the opening of the Call, updated drafts may be publihsed on the JU's website. The final content of these drafts may be agreed upon together with the relevant signatories.

The expression of interest for the selection of a Hosting Consortium will be evaluated by a group of independent experts[10] in accordance with the evaluation criteria set out in Section 5.

The selected Hosting Consortium may be eligible to receive the following two types of funding as long as its proposals for the three calls pass the necessary thresholds.

1.3.3.1 Funds for Joint Procurements – only for Hosting Entities

Joint procurements are managed by **Joint Procurement Agreements (JPA).** The JPA is an agreement between the Chips JU and the contracting authority of a Member State in order to set the rules to procure, in accordance with Article 165(2) FR, the tools and equipment from third-party vendors, that will be hosted by the Hosting Entity of that Member State.

It must be noted that there will be one JPA per Hosting Entity. This means that in a consortium with only one Hosting Entity there will only be one JPA while in a consortium with three Hosting Entities there would be one JPA for each Hosting Entity.

Given that in each JPA "*the share pertaining to or managed by the contracting authority of a Member State in the total estimated value of the contract will be equal to or above 50 %*" (Article 165(2) FR), the procedural rules applicable to the contracting authority of that Member State may apply to the joint procurement, provided that those rules may be considered as equivalent to those of the Union.

In this context, Member States have **two possible options** regarding who will act as contracting authority and therefore sign the JPA:

- **Option 1**: the joint procurement is carried out by the Member State in accordance with national procurement rules. In this case, given that the Member State itself will act as contracting authority, the JPA will be signed between the Chips JU and the Member State.

- **Option 2**: the joint procurement is carried out by the Member State, who decides to delegate the procurement process to the Hosting Entity established in that Member State, that will procure in the name and on behalf of the Member State. However, this option is only possible *as long as* the Hosting Entity can be considered a "contracting authority" within the meaning of the Procurement Directive[11]. In this case, the JU signs the JPA with the Hosting Entity, acting as contracting authority. The other members of the Hosting Consortium which are not Hosting Entity(ies) (i.e., do not have a hosting site with tools and equipment) may not in any event be signatories to the JPA and may not be involved in the procurement process.

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10 The group of independent experts that will evaluate the expression of interest for the selection of a Hosting Consortium may be the same group that evaluates the proposals for the Horizon Europe and Digital Europe Programme calls.

11 Directive 2014/24/EU of the European Parliament and of the Council of 26 February 2014 on public procurement and repealing Directive 2004/18/EC

In the abovementioned Model Letter of Intent, the Member State will have to indicate what option it intends to use and thus which entity it proposes as signatory of the JPA. In both cases, 50% of the procured tools and pieces of equipment of the pilot line shall be owned by the Chips JU. Regarding the remaining 50%, the Member State may decide to transfer its share of ownership to the relevant Hosting Entity.

1.3.3.2 Grants under the Horizon Europe and Digital Europe Programmes

As mentioned in Section 1.3.2, the present Call Document includes two calls for proposals for grants:

- **Set-up, integration and process development Grant**: this grant would cover the costs of deploying the infrastructure at a sufficient maturity level and the R&D&I activities required for the development of the process technology. This includes inter alia the cost to define tender specifications (for procurements), to integrate procured tools and equipment with existing facilities, to modify equipment, test, verify and validate the integration of the pilot line, and to develop the PDK/ADK (including its interfacing / deployment in the Design Platform). This grant will be established as a Horizon Europe Grant Agreement and will be evaluated according to Horizon Europe rules (See Section 5).

- **A Grant for the operational activities**: this grant would cover part of the operational activities of the pilot line, i.e., part of the standard operating costs of the pilot line. This grant will be established as a Digital Europe Programme Grant Agreement and will be evaluated according to the Digital Europe Programme rules (See Section 5).

Applicants must justify that no double funding is requested. Funding can only be provided on the condition that the prohibition on double funding is respected.

The proposals submitted to each of these calls and included in the application will be evaluated separately, possibly by the same group of independent experts. The results of these evaluations will be ranked lists.

EU funding rates are up to 50% for grants under the Digital Europe Programme, and up to 100% for grants under Horizon Europe.

1.3.3 The Hosting Agreement

On the basis of the abovementioned ranked lists, the Public Authorities Board (PAB) of the Chips JU will:

- Select the Hosting Consortium that will implement the pilot line;
- Award the grant for ‘Set-up, integration and process development’;
- Award the grant for the ‘Operational activities’.

A proposal needs to have passed the applicable thresholds in all three evaluations to be selected as the Hosting Consortium and to be awarded the above grants.

Subsequently, the coordinator and the Chips JU will sign a ***Hosting Agreement.*** The Hosting Agreement is the contract that lays down the rules that shall apply to the Hosting Consortium in the context of the implementation of the pilot line. The Hosting Agreement and the conditions described therein are valid until the end of 2031, and may be renewed subject to additional funding under the next MFF.

However, before the signature of the Hosting Agreement (but after the selection of the Hosting Consortium by the PAB), the Chips JU and the Hosting Consortium may address and finetune certain elements of the application. The final version agreed upon by the Chips JU and the Hosting Consortium will be the "Description of Action" which will be annexed to the Hosting Agreement and to the two Grant Agreements.

1.3.4 Responsibility and liability of the consortium

It must be noted that all members of a Hosting Consortium are jointly responsible for implementing the pilot line in line with the Hosting Agreement. To implement the action properly, they must make appropriate internal arrangements.

1.3.5 State aid

The fulfilment of State aid rules is a responsibility that pertains solely to the Member States. It is therefore their responsibility to assess whether the aid they intend to provide to the pilot line can be considered State aid and therefore potentially require a notification to the European Commission. Each case may be different and present similar but also slightly different characteristics.

2 OBJECTIVES

The overall objective of the present Call Document is to select a Hosting Consortium in order to implement the pilot line in line with Section 1.3.

The Pilot Line "Title of the pilot line" to be implemented is described below.

A key element of the pilot line is to serve as a bridge from the lab to the fab, by providing industry a facility to test, experiment and validate semiconductor technologies and system design concepts. Such testing and experimentation would allow industry actors to test technologies for the development of new or improved products and processes. While the pilot lines is not expected to offer fully matured fabrication services, its evolution is crucial in aiding industry to refine and advance its processing techniques and prototype next generation devices.

Furthermore, the pilot line must provide the facility for industry to characterise and evaluate advanced processes and potential outputs stemming from their process technology in collaboration with the Hosting Consortium and in line with the conditions, including those related to access, set out in this Call Document. The Hosting Consortium is required to specify the terms and conditions for any of the foreseen collaborations with industry.

To this end, the Hosting Consortium is required to submit an application with proposals for the three calls that takes into consideration collaboration with industry and other relevant stakeholders established in the Union – and where justified beyond – by credibly addressing several or all of the following elements:

- **Process development**: describe planned collaboration with equipment manufacturers in the development of next-generation equipment related to the process technology being developed on the pilot line.
- **Process technology**: provide a roadmap for the eventual transfer of elements or all of the process technology to industrial partners in their deployment of mass-production facilities.
- **Development**: list potential development, including collaborative development involving the Hosting Consortium, of prototype devices on the pilot line infrastructure. Additionally, include a detailed description of the assistance the Hosting Consortium offers to users of the pilot line.
- **Skills development**: give an overview of the plans for developing technical skills and operational know-how, particularly in relation to process development, process technology, and designing, creating, and refining semiconductor devices, and the anticipated spill-over effect of strengthening the European workforce to the benefit of European industry.
- **Research output**: provide an overview of all the expected research collaborations with industry, other RTOs, and academic institutions, and the foreseen outputs.

2.1 Description of the pilot line

The descriptions of the pilot lines are given in Sections 3.1-3.4 in the Work Programme part above.

3 BUDGET AVAILABLE

The Union financial contribution to the Chips JU for the implementation of the Pilot Line shall cover up to 50 % of the total costs of the pilot line. The remaining total cost of the pilot line (including VAT if applicable) shall be covered by the members of the Hosting Consortium and/or by the Participating State(s) where the Hosting Consortium members are established.

The total maximum EU budget is as follows:

- Joint procurements of equipment and tools: up to EUR XXX million from the Digital Europe Programme;

- Set-up, integration and process development: up to EUR XXX million from Horizon Europe;
- Operational activities: up to EUR XXX million from the Digital Europe Programme.
- Total pilot line: up to EUR XXX million.

The respective amounts for the pilot lines are given in Sections 3.1-3.4 in the Work Programme part above.

The sum of the EU budgets requested in the proposals for the three parts above (joint procurement, Horizon Europe grant, Digital Europe Programme grant) in an application may not exceed the total maximum EU budget above.

The Executive Director may adapt the amounts for the actions set out in Section 4 based on the amounts requested in the submissions received.

4 CONTENTS OF THE APPLICATION

An application must be submitted using the application form included as Annex 1 to this call. As indicated above, the application should include:

- An expression of interest for the Call for Expression of Interest for the selection of a Hosting Consortium for the pilot line;
- A proposal for the Call for Proposals (CfP) for Set-up, integration and process development (Horizon Europe);
- A proposal for the Call for Proposals (CfP) for Operational activities of the pilot line (Digital Europe Programme).

The application needs to contain the following information, amongst other potential considerations:

- **Detailed description and timeline**: An overview of the pilot line infrastructure, with details on the phased implementation approach of the project in terms of a *technology roadmap*. Furthermore, the proposal shall include a description of the major phases of the pilot line's development highlighting equipment acquisition, procurement timing, process development, integration, testing, validation, operationalisation and the possible development of demonstrators within the context of a work plan. Such a roadmap and work plan shall mainly include two phases:
  - a **development phase**, i.e., the procurement, set-up, engineering and integration efforts and process development required for preparing the pilot line to become fully operational (mostly relevant for the CfP for Set-up, integration and process development); and,
  - an **operational phase**, i.e., the efforts related to the access and service provisioning of the pilot line to the wider community of the pilot line (mostly relevant for the CfP for Operational activities).

- **Collaboration**: Each pilot line shall make an effort to have spill-overs beyond its immediate scope and involve a number of relevant stakeholders from across the Union (mostly relevant for the CfP for Set-up, integration and process development).
  - Collaboration with other pilot lines: by ensuring complementarity and, where possible, identify methods of amalgamation of activities.
  - Collaboration with RTOs and academia: by ensuring research partnerships with relevant research organisations thereby ensuring spill-over effects. Pilot lines should also strive to work with universities and training institutions in skills development.

- **Management of the distributed elements** of the pilot line (if any): The proposal needs to clearly explain the terms of collaboration between the different members of the consortium and shall provide a credible description of how distributed elements of the pilot line will work in synergy together as one pilot line in an efficient manner that enables European added value (mostly relevant for the CfP for Set-up, integration and process development).

- **Business model**: A description of the business model related to the functioning (i.e., service provisioning) of the pilot line, once it has been set up. The business model must outline a reasonable breakdown of the expected income via market-oriented access conditions. It should clarify how these revenues will contribute to covering a portion or the entirety of the operational expenses associated with the pilot line (mostly relevant for the CfP for Operational activities).

- **Access conditions**: Detailed description of the access conditions to be applied by the pilot line, based on the boundary conditions set by the legal acts, the work programme, and the international obligations of the EU (mostly relevant for the CfP for Operational activities). Furthermore, following Article 128(5) SBA Amendment, applicants are reminded of the following guiding principles:
  - Inclusivity: access to the facilities, resources, and expertise related to the pilot line should be available to a diverse range of users across the European Union. This inclusivity extends to stakeholders from academia, industry, research institutions, and any other entities that are interested in the pilot line.
  - Transparency: Information regarding the criteria, processes, and terms governing access to the pilot line shall be clear and transparent to ensure that potential users have a comprehensive understanding of the access framework.
  - Non-Discrimination: Access shall be granted on a non-discriminatory basis, avoiding preferential treatment of potential users based on their geographic location, affiliation, etc.

Furthermore, the following provisions need to be catered for:

- To further advance the principles outlined above, access to the pilot line by users established in the Union shall be directly proportional to the financial contribution made by the European Union to cover the costs of the proposed project.
- Recognising the role played by Small and Medium-sized Enterprises (SMEs) in driving innovation and economic growth, a Hosting Consortium needs to grant preferential access or reduced prices to SMEs, including startups, as well as to academic institutions. Applicants may establish a differentiated pricing structure

specifically tailored to accommodate the financial capacity of SMEs and academic institutes. This approach would facilitate the engagement of SMEs and academic institutions by ensuring that cost barriers do not impede their ability to access the pilot line. Access to the pilot line at preferential conditions for SMEs and academic institutions should be guaranteed until the duration of the Hosting Agreement, possibly after the end of funded activities.

- Applicants need to anticipate potential situations of excessive demand for access to the pilot line, putting in place mechanisms to ensure fairness, transparency, and equal opportunity for all interested parties. The proposal needs to establish clear procedures for managing and mitigating excessive demand, which may include collaboration with external partners, expansion of capacity where feasible, etc.
- In accordance with Article 5(b)(iii) Chips Act, the Hosting Consortium needs to provide support to integrated production facilities and open EU foundries through preferential access to the pilot line, as well as ensure access on fair terms for a wide range of users of the Union's semiconductor ecosystem.
- Access should be foreseen for international research and commercial partners (in line with Recital (18) Chips Act), in particular taking into account Union policies that affect the European semiconductor ecosystem, such as certain Digital Partnerships and Trade and Technology Councils.
- Access to the pilot line shall also be granted in relation to virtual assets, including but not limited to Process Design Kits (PDKs), Assembly Design Kits (ADKs), and their corresponding documentation, emanating from its development. Applicants need to elaborate on the methods by which such access will be realised and present the degree of openness of the access policy governing the diverse components of the PDK/ADK.

- **Procurement of equipment (CAPEX)**: The (rough) costings and technical specifications of each tool and piece of equipment that shall be procured from third-party vendors. It should also be indicated what costs fall within the scope of Article 129(4) of the SBA Amendment on retroactivity (mostly relevant to the Call for Expression of Interest).

- **Set-up, integration and process development (RDI activities)**: A description of the work required for the set-up, integration, and process development, as well as for the testing and validation of the process technology activities including costs until the pilot line is at a sufficient level of maturity such that it can be considered operational. Set-up and integration costs should be related to the corresponding piece of equipment (where relevant). This includes an overview of how the pilot line will be interfaced with the broader community through PDKs/ADKs, technology interfaces etc. The hosting consortium needs to ensure the availability of the PDKs/ADKs in the Design Platform and sufficient integration with relevant EDA tools.

- **Operational activities**: A description of the activities related to the operational phase of the pilot line (i.e., the service provisioning of the pilot line to the wider community), the expected engagement with third parties and an estimate of the costs and possible funding required for the satisfactory operation and use of the common infrastructure. Here, costs may include the expenses related to the operation of the heavy equipment and cleanrooms, i.e., maintenance, energy/electricity, personnel costs for running the pilot line. The

proposal needs to contain a business model that considers expected future revenues based on appropriately defined access conditions, explaining how such revenues will cover part or all of the pilot line's operational expenses.

- **Budget**: A detailed line-by-line breakdown of all costs that shall be categorised in three categories: (i) CAPEX; (ii) set-up, integration and process development costs; and (iii) operational costs. The proposal must include a distribution of the budget for the three categories over time, with a planning horizon of at least 5 years.

- **Exploitation plans**: Detailed exploitation plans for the pilot line beyond the period of financial support from the Chips JU (including potential support financed under the next MFF). These plans need to include:
  - A description clearly indicating the sustainability of the pilot line beyond what will be financed in the current MFF.
  - Prospective plans and costs for modification/extension of the pilot line's infrastructure beyond the current MFF, where applicable.
  - Prospective estimates for the costs for its operation / usage by third parties beyond the current MFF.

- **Synergies with the Chips Act**: Clarification of the links to the broader Chips for Europe Initiative activities, such as the Design Platform, Competence Centres, and skills development.

In addition to the above, any application submitted by the hosting consortium should be accompanied by **Letters of Intent** from the relevant public authorities of all Participating States supporting the Hosting Consortium and its application for a pilot line.

Such letters should specify the Participating States' financial commitments for the necessary national co-funding for the acquisition, set-up and integration, and operation of the pilot line. The letters should also define whether, in line with Article 165(2) Financial Regulation, the Member State in which a Hosting Entity is established[12] carries out the joint-procurement procedure itself (as contracting authority) or whether it delegates the procedure to the Hosting Entity. The latter case is only possible as long as the Hosting Entity can be considered a contracting authority within the meaning of the Procurement Directive. **The Letters of Intent must also specify clearly that the Member State supports that the Chips JU co-owns 50% of the tools and equipment of the pilot line.**

5 ADMISSIBILITY REQUIREMENTS

An application for the call for pilot line is not admissible if it has not been introduced under the 3 calls.

[12] Hosting Entities must be established in Participating States that are Member States

There are no page limits for the application but the consortia are encouraged to limit the narrative part of the application to 200 pages excluding the tables that are expected.

5.1 Admissibility requirements for the Call for Expression of Interest

To be admissible:

a) An application must be submitted no later than the **29 February 2024 at 17:00:00 Brussels time.**
b) An application must be submitted electronically (see section "Procedure for the submission"), using the application form in the Annex 1 (Chips JU Application Form)
c) An application must be submitted as described in Section 11;
d) The application is written in English.

Failure to comply with those admissibility requirements will lead to the rejection of the application.

Furthermore, the submitted application needs to be accompanied by the requested Letters of Intent from the Participating States supporting the Hosting Consortium.

5.2 Admissibility requirements for the Call for Proposals for Set-up, integration and process development

Admissibility conditions for this call follow the standard Horizon Europe admissibility conditions as stated in Annex A and Annex E of the Horizon Europe Work Programme General Annexes[13], with the exception of any page limits. Submission needs to follow the provisions in Section 11.

5.3 Admissibility requirements for the Call for Proposals for Operational activities of the pilot line

Proposals must be submitted before the call deadline **29 February 2024 at 17:00:00 Brussels time.**

Proposals must be complete and contain all the requested information and all required annexes and supporting documents and follow the Application Form.

At proposal submission, the coordinator will have to confirm that it has the mandate to act for all applicants. Moreover, the coordinator will have to confirm that the information in the

[13] https://ec.europa.eu/info/funding-tenders/opportunities/docs/2021-2027/horizon/wp-call/2023-2024/wp-13-general-annexes_horizon-2023-2024_en.pdf

application is correct and complete and that the participants comply with the conditions for receiving EU funding (especially eligibility, financial and operational capacity, exclusion, etc). Before signing the grant, each beneficiary and affiliated entity will have to confirm this again by signing a declaration of honour (DoH). Proposals without full support will be rejected.

The application must be readable, accessible and printable.

Applicants may be asked at a later stage for further documents (for legal entity validation, financial capacity check, bank account validation, etc).

6 ELIGIBILITY CRITERIA

6.1 Eligibility criteria for the Call for Expression of Interest

The call is open to entities or consortia of entities fulfilling cumulatively the following conditions:

a) The Hosting Consortium shall include the members that will host and operate the pilot line. The members of the consortium shall be from a Participating State to the Chips JU.
b) A consortium must consist of:
   (a) at least one independent legal entity established in a Member State; and
   (b) at least two other independent legal entities each established in a different Participating State;
c) The members of the Hosting Consortium shall be registered as a legal entity in one of the Participating States;
d) The applicant(s) shall have a legal personality on the date of the deadline for submission of applications and must be able to demonstrate their existence as a legal person.
e) Applications shall include the provision of appropriate supporting documentation proving for each member of the Hosting Consortium that the commitment of the Participating State(s) where the member(s) of the consortium is/are established will cover the share of the total cost of implementation of the pilot line that is not covered by the Union contribution referred to in Article 128 of the SBA.
f) Applications shall ensure, in accordance with Article 128(5) of the SBA Amendment, that access to the pilot line "*be open to a wide range of users across the Union and granted on a transparent and non-discriminatory basis directly proportional to the financial contribution by the Union to the total costs of those activities*".
g) Applications shall ensure, in accordance with Articles 13(4) and 14(5) of the Chips Act that integrated production facilities and open EU foundries "*have preferential access to the pilot lines […]. Any such preferential access shall neither exclude nor prevent effective access on fair terms to the pilot lines by other interested undertakings, in particular start-ups and SME*s"

In its application, the coordinator must be given a mandate to represent the other members of the Hosting Consortium to sign and administrate the Hosting Agreement and the various associated grants.

To assess the applicants' eligibility, the following supporting documents are requested:

- The legal entity identification form[14] duly completed and signed by the person authorized to enter into legally binding commitments on behalf of the applicant organization(s) to be submitted in original or a PIC number;

The following entities will be considered as non-eligible:

- natural persons;
- entities without legal personality.

6.2 Eligibility criteria for the Call for Proposals for Set-up, integration and process development

Eligibility criteria for this call follow the standard Horizon Europe eligibility criteria as stated in Annex B of the Horizon Europe Work Programme General Annexes[15].

6.3 Eligibility criteria for the Call for Proposals for Operational activities of the pilot line

Eligible participants (eligible countries)

In order to be eligible, the applicants (beneficiaries and affiliated entities) must:

- be legal entities (public or private bodies)
- be established in one of the eligible countries, i.e.:
    - EU Member States (including overseas countries and territories (OCTs))
    - non- EU countries:
        - EEA countries (Norway, Iceland, Liechtenstein)
        - countries associated to the Digital Europe Programme or countries which are in ongoing negotiations for an association agreement and where the agreement enters into force before grant signature.

Beneficiaries and affiliated entities must register in the Participant Register — before submitting the proposal — and will have to be validated by the Central Validation Service (REA Validation). For the validation, they will be requested to upload documents showing legal status and origin.

Moreover, participation in any capacity (as beneficiary, affiliated entity, associated partner, subcontractor or recipient of financial support to third parties) is limited to entities established in eligible countries.

[14] http://ec.europa.eu/budget/contracts_grants/info_contracts/legal_entities/legal_entities_en.cfm
[15] https://ec.europa.eu/info/funding-tenders/opportunities/docs/2021-2027/horizon/wp-call/2023-2024/wp-13-general-annexes_horizon-2023-2024_en.pdf

7 EXCLUSION CRITERIA

7.1 Exclusion criteria for the Call for Expression of Interest

There are no specific exclusion criteria for the Call for Expression of Interest. However, it must be noted that the exclusion criteria mentioned in sections 7.2 and 7.3 apply for the purpose of the award of the grants. Given that, as mentioned in Section 1.3.2, a consortium will only be eligible for funding if its proposal for all three calls passes the necessary thresholds, a hosting agreement cannot be concluded with entities which fall in an exclusion situation mentioned in sections 7.2 and/or 7.3.

7.2 Exclusion and selection criteria for the Call for Proposals for Set-up, integration and process development

Criteria related to financial and operational capacity and exclusion are described in Annex C of the Horizon Europe Work Programme General Annexes[16].

7.3 Selection and exclusion criteria for the Call for Proposals for Operational activities of the pilot line

Financial capacity

Applicants must have stable and sufficient resources to successfully implement the projects and contribute their share. Organisations participating in several projects must have sufficient capacity to implement all these projects.

The financial capacity check will be carried out on the basis of the documents applicants will be requested to upload in the Participant Register during grant preparation (e.g. profit and loss account and balance sheet, business plan, audit report produced by an approved external auditor, certifying the accounts for the last closed financial year, etc). The analysis will be based on neutral financial indicators, but will also take into account other aspects, such as dependency on EU funding and deficit and revenue in previous years.

The check will normally be done for all beneficiaries, except:

- public bodies (entities established as public body under national law, including local, regional or national authorities) or international organisations
- if the individual requested grant amount is not more than EUR 60 000.

If needed, it may also be done for affiliated entities.

[16] https://ec.europa.eu/info/funding-tenders/opportunities/docs/2021-2027/horizon/wp-call/2023-2024/wp-13-general-annexes_horizon-2023-2024_en.pdf

If the JU considers that your financial capacity is not satisfactory, it may require:

- further information
- prefinancing paid in instalments
- (one or more) prefinancing guarantees
  or
- propose no prefinancing
- request that you are replaced or, if needed, reject the entire proposal.

Operational capacity

Applicants must have the know-how, qualifications and resources to successfully implement the project and contribute their share (including sufficient experience in projects of comparable size and nature).

This capacity will be assessed together with the 'Implementation' award criterion, on the basis of the competence and experience of the applicants and their project teams, including operational resources (human, technical and other) or, exceptionally, the measures proposed to obtain it by the time the task implementation starts.

If the evaluation of the award criterion is positive, the applicants are considered to have sufficient operational capacity.

Applicants will have to show their capacity via the following information:

- general profiles (qualifications and experiences) of the staff responsible for managing and implementing the project
- description of the consortium participants
- list of previous projects (key projects for the last 4 years).

Additional supporting documents may be requested, if needed to confirm the operational capacity of any applicant.

Exclusion

Applicants which are subject to an EU exclusion decision or in one of the following exclusion situations that bar them from receiving EU funding can NOT participate[17]:

- bankruptcy, winding up, affairs administered by the courts, arrangement with creditors, suspended business activities or other similar procedures (including procedures for persons with unlimited liability for the applicant's debts)
- in breach of social security or tax obligations (including if done by persons with unlimited liability for the applicant's debts)

[17] See Articles 136 and 141 of EU Financial Regulation

- guilty of grave professional misconduct (including if done by persons having powers of representation, decision-making or control, beneficial owners or persons who are essential for the award/implementation of the grant
- committed fraud, corruption, links to a criminal organisation, money laundering, terrorism-related crimes (including terrorism financing), child labour or human trafficking (including if done by persons having powers of representation, decision-making or control, beneficial owners or persons who are essential for the award/implementation of the grant
- shown significant deficiencies in complying with main obligations under an EU procurement contract, grant agreement, prize, expert contract, or similar (including if done by persons having powers of representation, decision-making or control, beneficial owners or persons who are essential for the award/implementation of the grant
- guilty of irregularities within the meaning of Article 1(2) of EU Regulation 2988/95 (including if done by persons having powers of representation, decision-making or control, beneficial owners or persons who are essential for the award/implementation of the grant)
- created under a different jurisdiction with the intent to circumvent fiscal, social or other legal obligations in the country of origin or created another entity with this purpose (including if done by persons having powers of representation, decision-making or control, beneficial owners or persons who are essential for the award/implementation of the grant).

Applicants will also be rejected if it turns out that[18]:

- during the award procedure they misrepresented information required as a condition for participating or failed to supply that information
- they were previously involved in the preparation of the call and this entails a distortion of competition that cannot be remedied otherwise (conflict of interest).

7.4 Rejection from the Call

The Executive Director of the Chips JU shall not conclude a Hosting Agreement with a consortium where any applicants:

- is in an exclusion situation established in accordance with sections 7.2 and/or 7.3;
- has misrepresented the information required as a condition for participating in the procedure or has failed to supply that information.

The same exclusion criteria apply to affiliated entities.

Administrative sanctions (exclusion) may be imposed on applicants, or affiliated entities where applicable, if any of the declarations or information provided as a condition for participating in this procedure prove to be false.

[18] See Article 141 EU Financial Regulation

8 EVALUATION CRITERIA

8.1 Evaluation criteria for the Call for Expression of Interest

This Section explains the evaluation criteria for the CfEoI. Eligible applications will be evaluated according to the following evaluation criteria:

1. **Excellence and relevance**
    - *Clarity and pertinence of the pilot line's objectives, and the extent to which the proposed pilot line complies with the general specifications, is ambitious, and goes beyond the state-of-the-art while being relevant for the Initiative and the other components of the Chips Act.*
    - *Soundness of the proposed methodology, including the underlying concepts, models, assumptions.*
    - *Clarity and pertinence of the cooperation between the pilot line and the other actions under the Chips for Europe Initiative.*
    - *Clarity and pertinence of access conditions and their practical implementation, including the business plan for covering the operational expenses related to access to the pilot line.*

2. **Impact**

    The extent to which the outputs of the project shall contribute at the European and/or international level to:
    - *Credibility of the pathways to achieve the expected outcomes and impacts, and the likely scale and significance of the contributions.*
    - *Suitability and quality of the measures to maximize expected outcomes and impacts, as set out in the dissemination and exploitation plan, including communication activities.*
    - *Credibility of the business model justifying the sustainability of operating the pilot line beyond the end of the project.*
    - *Significant spill-overs that support the broader European semiconductor ecosystem.*

3. **Quality and efficiency of the implementation**

    The following aspects will be considered:
    - *Quality and effectiveness of the work plan, assessment of risks, and appropriateness of the effort assigned to work packages, and the resources overall.*
    - *Capacity and role of each participant, and the extent to which the consortium brings together the necessary expertise.*

    Experience of the Hosting Entity(ies) in implementing and operating similar systems;
    - *Quality and pertinence of experience of the Hosting Entity in installing and operating similar systems.*
    - *Extent that provided experience is sufficient for supporting the system described in the general system specifications.*

    Quality of the hosting facility's physical infrastructure and;
    - *Quality and pertinence of the current and proposed hosting facility's physical capacity and preparedness.*

Quality of service to the users, namely capability to comply with the service level agreement provided among the documents accompanying the selection procedure;

- *Quality and pertinence of service to the users, namely capability to comply with the service level agreement provided in the Hosting application.*
- *Quality of the proposed coordination and/or support measures to ensure requested service level towards pilot line users.*

Total cost of ownership of the pilot line and methodology to calculate it including an accurate estimate and a verification method of the set up and integration costs as well as the operating cost of the pilot line during its lifetime;

- *Clarity and effectiveness of the estimated cost of implementation of the application.*
- *Appropriateness of the methodology to calculate, report, validate and verify the operating costs.*

Criterion	**Maximum score**	**Threshold**
Excellence and Relevance	30	15
Impact	30	15
Quality and efficiency of the implementation including the Total Cost of Ownership	40	20
	100	60

Points will be allocated out of a total of 100 based on the table. Applications below these thresholds will be rejected.

8.2 Evaluation criteria for the Call for Proposals for Set-up, integration and process development

Award criteria for Research and Innovation Actions:

1. Excellence

- Clarity and pertinence of the project's objectives, and the extent to which the proposed work is ambitious and goes beyond the state of the art.
- Soundness of the proposed methodology, including the underlying concepts, models, assumptions, inter-disciplinary approaches, appropriate consideration of the gender dimension in research and innovation content, and the quality of open science practices, including sharing and management of research outputs and engagement of citizens, civil society and end-users where appropriate.

2. Impact

- Credibility of the pathways to achieve the expected outcomes and impacts specified in the work programme, and the likely scale and significance of the contributions from the project.
- Suitability and quality of the measures to maximise expected outcomes and impacts, as set out in the dissemination and exploitation plan, including communication activities.

3. Quality and efficiency of the implementation

- Quality and effectiveness of the work plan, assessment of risks, and appropriateness of the effort assigned to work packages, and the resources overall.
- Capacity and role of each participant, and the extent to which the consortium as a whole brings together the necessary expertise.

Scores and weighting

Evaluation scores will be awarded for the criteria. For full applications, each criterion will be scored out of 5. The threshold for individual criteria will be 3. The overall threshold, applying to the sum of the three individual scores, will be 10. There is no weighting.

Proposals that pass the individual threshold AND the overall threshold will be considered for funding, within the limits of the available call budget. Other proposals will be rejected.

8.3 Evaluation criteria for the Call for Proposals for Operational activities of the pilot line

The award criteria for this call are as follows:

1. Relevance
- Alignment with the objectives and activities as described in section 2
- Contribution to long-term policy objectives, relevant policies and strategies, and synergies with activities at European and national level

2. Implementation
- Maturity of the project
- Soundness of the implementation plan and efficient use of resources
- Capacity of the applicants, and when applicable the consortium as a whole, to carry out the proposed work

3. Impact
- Extent to which the project will achieve the expected outcomes and deliverables referred to in the call for proposals and, where relevant, the plans to disseminate and communicate project achievements
- Extent to which the project will strengthen competitiveness and bring important benefits for society

Evaluation scores will be awarded for the criteria. For full applications, each criterion will be scored out of 5. The threshold for individual criteria will be 3. The overall threshold, applying to the sum of the three individual scores, will be 10. There is no weighting.

Proposals that pass the individual thresholds AND the overall threshold will be considered for funding within the limits of the available budget (i.e. up to the budget ceiling). Other proposals will be rejected.

9 OVERVIEW OF THE EVALUATION AND SELECTION PROCEDURE

The Chips JU is responsible for the implementation of the evaluations of the received applications. It organises the submission and evaluation procedures and communicates with the applicants.

The following describes this process. It is the same procedure for the Call for Expression of Interest, for the Call for Proposals for Set-up, integration and process development, as well as for the Call for Proposals for Operational activities of the pilot line.

9.1 Evaluation procedure

The submitted applications will be evaluated in a procedure by a panel of seven independent experts. These experts will be appointed by the Chips JU on the basis of the procedure followed under Digital Europe Programme and Horizon Europe. This generic procedure to appoint experts will be as well used for the Call for Expression of Interest. For the applications considered admissible according to Section 5, the Chips JU will assess the eligibility and exclusion criteria according to Sections 6 and 7 above. Only admissible and eligible applications will be evaluated.

- **Individual evaluations**: In the first step, the independent experts that sit on the panel shall carry out individually the evaluation of the applications based on the evaluation criteria described in Section 5 above. They give a score for each criterion, with explanatory comments. These individual reports form the basis of the further evaluation.
- **Consensus meetings**: After carrying out their individual assessment, all the experts that evaluated the applications shall convene in a consensus meeting, to agree on a common position, including comments and scores and prepare a consensus report. The consensus meetings shall be moderated by a Senior Programme Officer of the Chips JU who shall seek consensus, impartially, and ensure that all applications are evaluated fairly, in line with the relevant evaluation criteria.
- **Panel review**: The review panel shall be chaired by the Executive Director of the Chips JU. The panel will review the scores and comments for all applications to check for consistency across the evaluations. If necessary, it will propose a new set of marks or revise comments, and resolve cases where evaluators were unable to agree. The panel will prepare a final evaluation summary report.

9.2 Selection

The Executive Director of the Chips JU will review the results of the evaluation panels and will elaborate final ranking lists for each evaluation, based on the lists proposed by the panels.

This final ranking list shall consist of:

– a main list with the applications to be selected by the experts;
– a reserve list, with applications that have passed the evaluation thresholds.

In addition, the Chips JU will prepare a list with applications that did not pass the evaluation thresholds or were found to be ineligible.

A consortium will only be eligible for funding if its application submitted to all three calls passes the necessary thresholds.

The Executive Director will submit the final ranking lists, together with the Evaluation Summary Reports, to the Public Authorities Board of the Chips JU with a proposal for selection of the application, for approval by the Public Authorities Board.

The Public Authorities Board will make the final selection of a consortium whose proposals were selected from submissions to the Call for Expression of Interest for the selection of a Hosting Consortium, the Call for proposals for the Set-up, integration and process development grant funded under the Horizon Europe Programme, and the Call for proposals for the operational activities of the pilot line, funded under the Digital Europe Programme. This consortium is the selected Hosting Consortium.

The Pilot Line will be implemented by one selected Hosting Consortium or not at all. The proposals submitted by the selected Hosting Consortium to the three calls are therefore selected.

After the decision of the Public Authorities Board, all applicants will be informed in writing by the Chips JU of the outcome of the evaluation in the form of Evaluation Summary Reports (ESR). The Chips JU will also inform about the final selection or rejection of applications.

The Chips JU will invite the coordinator of the selected Hosting Consortium to sign a Hosting Agreement with the Chips JU and to initiate grant agreement preparations. Grant agreements will only be concluded subject to the signature of the Hosting Agreement.

9.3 Communication

The information contained in the present call document provides all the information required to submit an application. Please read it carefully before doing so, paying particular attention to the priorities and objectives of the present call.

All enquiries must be made by e-mail only to: calls@chips-ju.europa.eu

Questions shall be sent to the above address no later than the **21 February 2024 17:00 Brussels time**, defined as "Deadline to submit questions about the Call" in Section 10.

The Chips JU has no obligation to provide clarifications to questions received after this date.

Replies will be given/published no later than the "Publication of the last answers to questions" defined in the timeline in Section 10.

To ensure equal treatment of applicants, the Chips JU will not give a prior opinion on the eligibility of applicants, or affiliated entity(ies), an action or specific activities.

No individual replies to questions will be sent but all questions together with the answers and other important notices will be published (FAQ in EN) at regular intervals on the website under the relevant call: https://www.chips-ju.europa.eu/initiative/.

The Chips JU may, on its own initiative, inform interested parties of any error, inaccuracy, omission or clerical error in the text of the Call Document on the mentioned website. It is therefore advisable to consult this website regularly in order to be informed of any updates and of the questions and answers published.

No modification to the applications is allowed once the deadline for submission has elapsed. If there is a need to clarify certain aspects or to correct clerical mistakes, the Chips JU may contact the applicant for this purpose during the evaluation process. This is generally done by e-mail. It is entirely the responsibility of applicants to ensure that all contact information provided is accurate and functioning.

In case of any change of contact details, please send an email with the application reference and the new contact details to [insert email address].

In the case of hosting consortia, all communication regarding an application will be done with the coordinator only, unless there are specific reasons to do otherwise, where the consortium coordinator shall be in copy.

Applicants will be informed in writing about the results of the selection process. Unsuccessful applicants will be informed of the reasons for rejection. No information regarding the award procedure will be disclosed until the notification letters have been sent to the relevant applicats.

10 TIMETABLE

The steps and indicative times for the procedure from publication to expected start of the mandate for the selected Hosting Consortium are in the table below:

Selection of Hosting Consortium milestones	Date and time or indicative period
Call Document Publication	
Publication of this Call Document	01-12-2023
Submission of applications	
Calls Deadline	29-02-2024 - 17:00
Application Opening day (open of envelopes with expressions of interest)	
Evaluation	TBD 22 March 2024
Selection by Public Authorities Board	26.03 2024
Notification of results to applicants	
Signature of the hosting agreement	April 2024
Signature of hosting agreement	
Signature of grant agreements	

This schedule is common to the three interrelated calls: publication, submission, evaluation and selection dates are the same.

The time table for the conclusion of the grant agreements are same for the HE and DEP calls:

Information on the outcome of the evaluation	Maximum 5 months from the final date for submission
Indicative date for the signing of grant agreements	Maximum 8 months from the final date for submission

11 PROCEDURE FOR THE SUBMISSION OF APPLICATIONS

11.1 For the Call for Expression of Interest

Applications must be submitted no later than the 29 February 2024 at 17:00 Brussels time. Application forms are available at https: https://www.chips-ju.europa.eu/initiative/

Applications must be submitted in the correct form, duly completed and dated. They must be submitted in electronic copy on https://www.chips-ju.europa.eu/Form-files/ and signed by the person authorised to enter into legally binding commitments on behalf of the applicant organisation. The electronic version must contain the pdf versions of the application presented

in paper and other files such as list of equipment (EXCEL spreadsheet), List of costs (EXCEL spreadsheet), etc.

Contact point for any questions[19] is calls@chips-ju@europa.eu.

11.2 For the Call HE

Applications submitted to EU funding & tender portal.

11.3 For the Call DEP

Applications submitted to EU funding & tender portal.

11.4 Other submission related comments

All applications will be treated confidentially, as well as any submitted related information, data, and documents. The Chips JU will ensure that the process of handling and evaluating applications is carried out in a confidential manner.

External experts are also bound by an obligation of confidentiality.

Applicants shall avoid taking any actions that could jeopardize confidentiality. They must not attempt to discuss their application with persons they believe may act as expert evaluator for the Chips JU.

Your application shall not contain any information that is 'EU classified' under the rules on security of information in the Commission security rules for protecting EU classified information (see also Classification of Information in DEP projects).

The Chips JU will process personal data in accordance with Regulation (EU) 2018/1725 on the protection of natural persons with regard to the processing of personal data by the Union institutions, bodies, offices and agencies and on the free movement of such data, and repealing Regulation (EC) No 45/2001 and Decision No 1247/2002/EC9.

Once the coordinator (or sole applicant) has submitted an application, an acknowledgement of receipt will be sent by the JU. No other interaction will take place with the Chips JU until the application has been evaluated, unless the Chips JU needs to contact you (usually through the coordinator) to clarify matters such as eligibility or to request additional information.

END OF THE CALL FOR PILOT LINE DOCUMENT

[19] Questions on submission must be sent before the deadline indicated in Section 8.

Annexes

Annex 1	Application form template
Annex 2	Draft Model Hosting Agreement
Annex 3	Draft Model Joint Procurement Agreement
Annex 4	Model Letter of Intent describing the formal commitment of each Participating State to financially support the pilot line and its participating Consortium members
Annex 5	HE model grant agreement for the R&D activities of the pilot line
Annex 6	DEP model grant agreement for the operational activities of the pilot line