Outline for the Chips JU Working Programme 2026

Version 3.02

Preamble

The business we are in.

ECS-business (wide definition) is expanding rapidly, already no.4 largest sector in the world, going to no.2 position, surpassing chemistry and automotive (two industries where Europe still has a top position and is at the basis of our welfare).

ECS business might grow to $1.900 billion by 2032 from $695 billion in 2024 (Fortune business insights)

Europe accounted for merely 9% of world semiconductors business in 2020 and it is expected that this might grow to 11,7% by 2030 ("Microchips: EU off the pace in a global race", European Court of Auditors, April 28th 2025)

AI data-centre energy consumption predicted to grow by 45% CAGR.

Usage of ECS has become the backbone of about anything on earth (defence, industry and energy, transport, communications, customer electronics, health…). In geopolitics semiconductors have become of prime importance and may on short notice become number one.

Expanding scope.

Regardless digital CMOS still is, by far, the prime technology, mixed analog-digital, power-electronics, AI & neuromorphic, photonics, quantum, … are broadening the scope. Systems-of-systems, advanced packaging, chiplet and chiplet architecture have become prominent aspects of innovation.

Innovation is no longer a stand-alone, but multidisciplinary. From logic and memory, a vast expansion into 'smart' sensors, imagers, actuators… has become the new reality

Automation and artificial intelligence are the powerful drivers in automotive, industrialisation, data-infrastructure, telecommunications, aerospace and defence, health and, with the emergence of technology like LLM, … into ordinary life.

Main drivers have become energy consumption and accommodating the novel potential of Artificial intelligence.

The business Chips JU is in.

Whereas the joint Undertakings ENIAC, ARTEMIS, ECSEL and KDT where there to strengthen industry in a genuine tripartite collaboration, the Chips JU has lifted the scope. It has taken the mission to grow the market share of Europe's industry and to prepare Europe for a future in which ECS presence is going to be potentially even more important to what chemicals and refined oil products have been in the past.

With the Chips Act the programme has doubled into a 'Chips for Europe initiative' and a 'Electronic Components and Systems initiative'. Whereas the latter has the ambition to capitalise and expand on the former successes of what tripartite joint undertakings accomplished, the first one is about a backbone of instruments that should help Europe in the

next future through pilot lines, design platforms, competence centres for networking, structures to enhance skills and steps in a still industrial far away future (e.g. Quantum).

Chips JU ECS: status.

One can structure into five fields of interest: photonics, telecom, health, automotive and artificial intelligence. Those fields already are a mixture of verticals and technologies. In the past all fields have been part of generic IA and RIA calls. On top of that, focus topics have been used to obtain strategic alignment.

In 2024 (first year of Chips JU) focus topics were launched on telecom (6G), Edge AI, control systems for energy supply, automotive autonomous driving. Focus topics accounted for somewhat 26% of the ECS budget.

In 2025 three focus topics are launched. Heterogenous integration of high-performance computing for automotive, a RISC-V automotive hardware platform and AI-assisted methods and tools for engineering automation, all of them as innovation actions. They account for 52% of the IA and RIA spending ECS in 2025.

In the project assignment the field of automotive has been the one with the highest alignment this far.

The Chips for Europe Initiative: status.

The initiative has been structured in five different topics: open lab infrastructure (pilot lines), design, networking, quantum and skills.

Pilot line infrastructure at the service of Europe: four initiatives funded and started in set-up, one pilot line in final grant negotiations has been the result of the work done in 2024. In 2025 follow-up actions on these initiatives, being SSOI and Lab-to-Fab, will be under grant negotiations.

Design acceleration consisting of a cloud enabled EDA platform and a coordination team for deployment and management have been selected. First local design enablement teams for further support have started. Open-source EDA tools initiatives have been selected. Additional funding (SME-targeted) has been set-up to be enabled as of 2025.

In networking 27 competence centres have been selected in 25 states (member states and one associated state). A smaller wave competence centres will be added, seeing all member states to a networking entity except for Iceland.

On quantum six consortia on six different quantum platforms have been selected under an FPA-call and SG-calls will be launched on each of them.

On skills, the initiatives and projects have been largely outside the Chips JU and part of DEP-calls. Projects and actions within the Chips JU will be guided and supported by the competence centres.

Current agreed plans for 2025 calls are primarily directed at getting SMEs and start-ups involved with over half of the budget (excluding CSAs and cloud platform). A lab -to-fab accelerator, to capitalise on the pilot lines and directed to support automotive with 12%, quantum chip technology with 17% and advanced strained silicon on insulator substrates (single grant) with 7,5% are the headlines of the program decided.

Structural expectations and limitations.

The resources of the Chips Joint Undertaking are already largely depleted. What is currently left to be assigned in the next two years (approximately):

- Chips for Europe Initiative: approximately €257M + approximately €55M 'Quantum' (based on the full launch of six SGAs)
- ECS: approximately € 327M

Taking "Microchips: EU off the pace in a global race", European Court of Auditors, April 28th 2025 into account, workplan 2026 and 2027 should put emphasis on measurable European industrial impact. More attention to the impact description of projects is advised.

Facing the new Multi Financial Framework there needs to be an appealing reason to capitalize on and continue a tri-partite collaboration with elevated funding.

Whereas industry makes an appeal to have more entirely open initiatives, Commission is requesting for more alignment and strategy.

Member states are requesting for more structure and the avoidance of some crooked situations like 'on ticket lottery' focus topics.

There is doubt on too large projects and consortia in their effectiveness and potential to be managed in a focussed manner to the Chips JU objectives.

The Chair of the Governing Board has requested to reduce the number of calls to prevent scattering and to reduce the administrative effort for the Chips JU office.

Political views of the Semiconductor Coalition to be presented at the European Semiconductor Board of June 24th are working according three principles (*Prosperity, Indispensability, Resilience)*. The indispensability encompasses the European unique offering in materials and equipment.

At the side of industry, efficiency and cost efficiency are prime, including the evaluation process. There is the suggestion to limit the number of projects going from project outline to full proposal. A cut-off passed PO, based on the PO-score, rather than on threshold, is suggested. It would reduce both FPP preparation by consortia as well as evaluation work at Chips JU office. Less stringent might be that upon PO-review, projects are given a recommendation green or orange, indicating that applying at FPP has a serious risk of not being selected. Prior art from other European programmes can be taken into consideration to help towards an efficient selection methodology going from PO to FPP.

Starting points

The outline gives a direction for the further development of the Work Programme by the Executive Director. Topics mentioned in the outline should be discussed for inclusion in the final version of the Work Programme. This does not mean that every topic in the outline must make it into the final version of the WP, or vice versa that every topic in the final version of the WP must have been mentioned in the outline. It follows that more topics may be mentioned in the outline than may be included in the final version of the WP. This allows for subsequent refinement and prioritisation.

As the AWP contains both Initiative and ECS, topics should be allocated to one of the two parts. The Initiative part comes with certain conditions, in particular topics need to contribute to the objectives of the Initiative and need to conform to rules of the programme (Horizon Europe or Digital Europe) that funds them. There is a certain flexibility in the allocation of topics to the Initiative or the ECS parts, i.e. certain topics could be reasonably considered for both parts, and final allocation may depend also on factors such as budget availability.

It is imperative to discuss what we want before discussing how much investments we deem necessary. Any indication of budget structuring is secondary to the content discussion.

Whereas the outline is probably not the place to indicate figures for the expected number of projects under a topic, expected or maximum project costs, expected or maximum project participants, …, practice in the past years shows that in particular expected project costs / EU contributions are insufficiently considered in AWPs. Therefore, the sooner these points are considered, the better. Expected or maximum project participants should ideally not be mentioned in AWPs at all, but experience in this JU shows that this may be necessary in certain cases.

The outline is to be considered as guiding and is not restricting. The AWP2026 may therefore deviate in any of its aspects.

Structuring the ECS calls.

Taking the limited resources left, an overall funding budget for AWP-2026 is +/- € 160M. In a first rough approach, one may split this into RIA, ‘IA indispensable’, ‘IA resilience’ and CSAs.

There has even been the request by some member states to pay attention to some low-TRL projects, as some Cluster 4 topics were to be accommodated in the (KDT &) Chips Joint Undertaking.

Overall initial funding structure would be:

- CSAs
- RIA including low TRL
- IA prosperity
- IA resilience

Not allocating budgets already, some outline for guidance is appropriate. An RIA:IA ratio in the direction of 1:2 rather than 1:3 is recommended.

CSA & International:

The number of CSAs and size should be limited. Suggested topics this far:

- International cooperation

  A potential joint R&I call with Taiwan (Chinese Taipei) could be launched, subject to political agreement. Taiwan's research community, including its universities and RTOs, brings complementary expertise in areas such as advanced packaging, heterogeneous integration, and photonic chip technologies. The call could focus on low-TRL research in chip design and manufacturing and would be aligned with the forthcoming Digital Dialogue at service level A possible joint R&I call with Taiwan (Chinese Taipei) could be considered if there is political agreement. Such call could cover low-TRL research on chip design and manufacturing and would be linked to the Digital Dialogue that is planned to start with Taiwan at service level.

- Supply chain resilience
  - A platform/database, gathering supply chain data from companies (similar to an extended semiconductor manufacturing data space to cover the full supply chain) that could be a natural successor to the SC4EU project.
  - A digital twin platform for semiconductor manufacturing covering the full supply chain. Stress tests risk analysis of the EU semiconductor supply chain.
- Global trustworthiness
  - Global traceability of integrated circuits has been a subject on several forums (G7 being one of them). The topic might be recommended for an in-depth view.

RIA including low TRL

- The RIA should enable a scope of broad new technologies and verticals. Project budget size is recommended not to exceed € 25M (typically €15M) with a recommended participant number of 20. This should enable about 7 projects being selected.
- One or two low TRL projects with a budget under € 5M could be given priority if their overall score is within one point of deviation of the average selected projects. This is to stimulate early-stage novel (smaller) initiatives and live up to the Cluster 4 to Chips JU shift that was initially intended.

IA prosperity

- The IA-prosperity call should focus on maintaining Europe's leading position where there is either a unique offering or in which Europe is clearly a market leader.
- The funding allocation should enable the selection of at least two projects. Recommended (but not limited) project budget size of € 50M. Funding claim might be typically €15M and is recommended not to exceed €23M. The number of participants is recommended not to exceed 30. Normal IA-funding percentages (20%LE, 25%SME, 35% RTO) are recommended, stressing the fact that applicants can reduce their claims to fit maximum funding ceilings.

IA resilience

- The IA-resilience call should focus on strengthening Europe in which there is no unique offering but in which Europe could keep or gain a competitive or leading position.
- To guide towards resilience and have European strategic alignment, a limited number of topics (three or four is suggested) should be open for major contributions to this call. Some suggestions for major topics are:

    - Photonics
        - Potential calls may focus on speeding up applications of technologies promoted by this pilot line, e.g. component development for 300 mm wafer production of photonic integrated circuits and thermal infrared imagers.
        - Here, an emphasis on sectors could be given, e.g. health or telecommunications.
    - Chips for AI / Edge Data Centres

      An important initiative would be to support the design of AI chips for edge datacentre applications to enhance EU's technological sovereignty. The focus should be on near-term deployment. This would need to complement existing actions in RISC-V development.

    - Telecom, digital industry, connectivity and energy

      Specific emphasis could be on the e.g. design of AI chip for 6G.

    - Health / Medical Devices.

      It is suggested that if 'telecom' is selected in 2026, 'health' would be in 2027 or vice/versa

    - Power electronics

      Capitalizing on Europe's competitive position in silicon power and capitalizing on the current position in the vastly expanding III-V power devices

- The funding allocation should enable the selection of at least four projects. Recommended (but not limited) project budget size of € 50M. Funding claim might be typically €15M and is recommended not to exceed €20M. The number of participants is recommended not to exceed 30. Normal IA-funding percentages (20%LE, 25%SME, 35% RTO) are recommended, stressing the fact that applicants can reduce their claims to fit maximum funding ceilings.

- One or two low small bottom-up projects with a budget under € 10M could be given priority if their overall score is within one point of deviation of the average selected projects. This is to stimulate development where primarily European interaction is prosperous (e.g. global authentication).

Structuring the Chips for Europe Initiative calls.

AI Compute for Sovereign Cloud (topic shared with ECS)

- Support the development of end-to-end AI compute solutions for datacentre and cloud platforms, encompassing high-performance AI SoCs, ultra-low-latency optical networking and a complete software stack, targeting near-term deployment in European infrastructure. By co-optimising hardware and software for industry-specific applications, these solutions will deliver optimal performance, efficiency, and scalability for different compute platforms. The aim is to reduce reliance on non-EU providers by developing energy-efficient, scalable architectures for AI workloads. A staged funding model could be explored, possibly in collaboration with the EIB, allowing smaller projects to demonstrate feasibility before scaling up.

Design Platform

- A new call will be used to select additional DETs. This also depends on the outcome of the first DET call.
- Additional topics may be considered to populate the Design Platform with generic IP and resources that can be used by start-ups, SMEs, and others. This includes software IP. AI chip companies would be prime suspects to define the requirements for this IP. Efforts are needed to raise the maturity of IP blocks. The exact contents of a topic could be defined progressively.

Scaling Advanced Photonic Technologies (topic shared with ECS)

- Ensuring Europe's technological leadership in photonics requires accelerated industrial uptake. This topic will support projects aimed at maturing advanced photonic technologies into commercially viable solutions, with a strong emphasis on integration into industrial-scale production. Projects should aim to achieve tangible improvements in industrial capacity, thereby enhancing European competitiveness, strengthening strategic autonomy in key photonic components, and securing resilient supply chains.

Skills, Outline

- To scale successful skills initiatives, a dedicated call could be envisaged to support local actions through the Chips Competence Centers. Such a call would enable consortia to propose skills development activities that build upon and complement the services offered by Chips Competence Centers, tailoring them to address specific national/regional needs.
- Proposed initiatives should focus on key areas including chip design, AI chips, manufacturing, advanced packaging, photonics, and quantum technologies. Emphasis should also be placed on vocational training for the photonics and microelectronics

industries, as well as reskilling programs for professionals transitioning from other industrial sectors with a surplus workforce.

- Here a first analysis may need to be carried out to determine to what extent skills activities are already covered by the Competence Centers, and where complementary activities could be envisaged.

Sustainable Manufacturing

- A potential co-financed call with IAM4EU to support the development of alternative materials and processes, enhancing sustainability and supply chain resilience in semiconductor manufacturing.

Quantum chips

- Quantum-specific design-related activities: supporting the development of tools, methods, and reusable components tailored to the needs of quantum chip design. Given the current fragmentation and immaturity of the quantum design landscape in Europe, the aim would be to enable progress on key elements such as simulation and verification environments, scalable error correction architectures, hybrid quantum-classical co-design flows, and initial platform-specific design libraries. Activities could include the creation of reusable IP blocks and support for early-stage design automation, facilitating more efficient design cycles and helping European research teams and start-ups make better use of multi-project wafer runs. Rather than attempting to cover the full quantum design stack, this topic would target specific areas where design bottlenecks are most acute and where there is potential for consolidation and reuse across different platforms.
- Enabling technologies that underpin the operation and scalability of quantum systems. These technologies, which support functions such as control, read-out, shielding, and thermal management, are essential for translating laboratory-scale setups into manufacturable, reliable systems. The topic could cover key components such as (cryogenic) electronics, low-noise amplification, cryostats and cooling infrastructure, packaging technologies, and interconnects.