Appendix 6

APPENDIX 6: ACTIVITIES LAUNCHED IN 2025 FOR THE CHIPS FOR EUROPE INITIATIVE PART

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CONTENTS

1 ACTIVITIES 2025 CHIPS FOR EUROPE INITIATIVE PART

This appendix foresees the launch of the following call topics with an estimated EU expenditure of as below:

HE ACTIONS		
Call Topics		
Topic	**Description**	**Indicative EU budget M€**
HORIZON-JU-Chips-2025-CSA	Pan-European infrastructure for Chips Design Innovation	**12**
HORIZON-JU-Chips-2025-IA-EDA	Open-source EDA tools development	**20**
Other actions not subject to calls for proposals		
HORIZON-JU-Chips-2025-RIA-SUP	Support for start-ups and SMEs	**220**
HORIZON-JU-Chips-2025-QAC1-1-SGA	Supporting developing Quantum Chip Technology for superconducting stability Pilot	**25**
HORIZON-JU-Chips-2025-QAC1-2-SGA	Supporting developing Quantum Chip Technology for photonic stability Pilot	**25**
HORIZON-JU-Chips-2025-QAC1-3-SGA	Supporting developing Quantum Chip Technology for semiconducting stability Pilot	**25**
HORIZON-JU-Chips-2025-QAC1-4-SGA	Supporting developing Quantum Chip Technology for diamond-based stability Pilot	**25**
HORIZON-JU-Chips-2025-QAC1-5-SGA	Supporting developing Quantum Chip Technology for neutral atoms stability Pilot	**25**
HORIZON-JU-Chips-2025-QAC2-SGA	Supporting developing Quantum Chip Technology for high-quality Trapped Ions Pilot	**25**
DEP ACTIONS		
Call Topics		
Topic	**Description**	**Indicative EU budget M€**
DIGITAL-JU-Chips-2025-CSA-DET	Set-up and integration of Design Enablement Teams	**5**
DIGITAL-Chips-2025-1-IA-LEAI	Low-power Edge AI Chips	**20**
DIGITAL-JU-Chips-2025-SG-SSOI	Accelerator for Advanced Strained Silicon on Insulator Substrates	**30**
DIGITAL-JU-Chips-2025-SG-LFA	Lab to Fab Accelerators for Advanced Packaging and heterogeneous integration	**50**
DIGITAL-JU-Chips-2025-CSA-LFA	Lab to Fab Accelerator ecosystem - Coordination and Support Actions. Boosting cooperation for industrial implementation on	**2**

	advanced packaging of chiplets and heterogeneous integration in Europe	
Other actions not subject to calls for proposals		
Topic	**Description**	**Indicative EU budget M€**
Call for tenders	Cloud platform for the European Design Platform	**15**
TOTAL		**424**

2 NATIONAL BUDGETS FOR THE INITIATIVE CHIPS FOR EUROPE INITIATIVE CALLS 2025

Participating states	Chips-2025-CSA-DET	Chips-2025-RIA - SUP	Chips-2025-IA-LEAI	Chips-2025-IA-EDA	Chips-2025-CSA	Chips-2025-SG-SSOI	Chips-2025-SG-LFA	Chips-2025-SGA-QAC1-1	Chips-2025-SGA-QAC1-2	Chips-2025-SGA-QAC1-3	Chips-2025-SGA-QAC1-4	Chips-2025-SGA-QAC1-5	Chips-2025-SGA-QAC2	Total (M€)
AT				0.5		1.0	3.0	1.0	0.9		2.92	4.0	12.0	24.82
BE-FL							3.0	7.0						10.0
BE-BR														
BE-WL														
BG														
CH														
CY														
CZ			0.25			0.35								2.1
DE				3.5		10.0	10.0							23.5
DE TH														
DE SN														
DK						7.3[1]								25.8[2]
EE														
EL														
ES AEI			0.5	0.5		0.5	0.5							2.0

[1] Budget shared between the calls DIGITAL-JU-Chips-2025-SG-LFA; DIGITAL-JU-Chips-2025-SG-SSOI; Electronic Components and Systems actions and Chips for Europe Initiative actions of 2026

[2] 18.5 M€ budget shared with Electronic Components and Systems actions launched in 2025, remaining 7.3 M€ shared as detailed in the footnote above.

ES MAETD														
FI	1.0						4.0	17.0						22.0
FR						10.5								35.5
HR														
HU														1.15
IE								1.12						1.12
IL														
IS														
IT MIMIT				2.0										2.0
IT MUR														
LT														1.0
LV														
LU														
MT														
NL			0.99			3.2		6.65	10.5	2.4				23.74
NO								2.0						2.0
PL														
PT														6.0
RO														
SE				0.34			0.42					0.18		0.95
SI														
SK							0.8							1.1

TR														
UK														
Total														184.78

3 TECHNICAL DESCRIPTION OF THE CALL TOPICS

In addition to the application of Article 22(5) of the Horizon Europe Regulation[3] (HE) to the relevant topics of the Chips JU's work programme, in line with Article 23 of the Single Basic Act, in order to ensure a coherent application of Article 22(5) HE, as well as Union legislation and guidance application in similar topics in the work programme of the Chips JU, eligibility of participants in a proposal submitted to a Call for Proposals for any of the topics in this work programme will take into account any application of Article 22(5) of HE triggered for topics from other HE Work Programmes (including the Chips JU's work programme) for calls for proposals with similar scope. This may be of particular relevance to proposals submitted to bottom-up RIA/IA topics, i.c. topics HORIZON-JU-Chips-2025-IA and HORIZON-Chips-2025-RIA, where despite the fact that Article 22(5) HE might already be used, stricter conditions may apply in case those proposals address areas covered under other HE work programme topics with a stricter application of Article 22(5) HE.

3.1 Design Platform

Semiconductor circuit design involves the development of integrated circuits (ICs) and system-on-chips (SoCs) by defining the functionalities and specifications of chips, capturing a significant share of the value within the semiconductor supply chain. The industry is increasingly shifting towards more complex, application-specific, and highly integrated semiconductors, making state-of-the-art design essential for competitiveness and differentiation across various applications. In this evolving landscape, fabless companies are uniquely positioned to lead technological innovation and address the demands of diverse applications, further solidifying their critical role and driving growth within the semiconductor sector.

The Chips Act underscores the strategic importance of fostering chip design growth in Europe to enhance the competitiveness of the Union's semiconductor industry. Pillar I of the Chips Act, the Chips for Europe Initiative, outlines an ambitious plan to strengthen the Union's resilience in semiconductor technologies, including promoting the growth of fabless companies focused on leading-edge technologies. This is especially pertinent given that the European share of global fabless semiconductor companies' revenues has shrunk to critically low levels, highlighting the urgent need for strategic initiatives to bolster this sector and enhance Europe's competitiveness. A critical mass of fabless companies is also key to generate further demand that would justify increased investment in semiconductor manufacturing capacity in Europe.

Recognising the Union's limited fabless capacity, and the significant barriers to entry in chip design, the Design Platform focuses on nurturing emerging companies in the sector. The Design Platform is at the heart of the Chips for Europe Initiative and is envisaged as a key

[3] Regulation (EU) 2021/695 of the European Parliament and of the Council of 28 April 2021 establishing Horizon Europe – the Framework Programme for Research and Innovation, laying down its rules for participation and dissemination

instrument to foster the development of a strong design ecosystem in the Union by creating a pipeline of highly innovative European fabless companies, focusing particularly on the growth of start-ups and SMEs.

In 2024, the Chips Joint Undertaking launched a call for the selection of a Platform Coordination Team (PCT). The selected PCT should assist the Chips JU in defining the technical specifications of a cloud service for the platform to be procured by the Chips JU through a dedicated Call for Tenders. This cloud infrastructure should incorporate all the services necessary for the efficient implementation of the Design Platform including repositories, a user authentication service, license usage monitoring and any relevant *Infrastructure as Code* to be deployed at the various Design Enablement Teams (DETs).

The PCT will be complemented by a number of DETs that should set up a cloud-based environment for users designing on the platform, support them in their design cycle, and facilitate access of users to foundry services. Furthermore, the DETs should be responsible for providing access to foundry services. In fact, it should be a pre-requisite that for an entity to become a DET, it must act as, or be linked to, a foundry aggregator.[4]

These DETs may be design houses and RTOs with the necessary expertise and experience in providing such services. They can be spread geographically but may also have different sectoral (e.g. defence) or technological (e.g. digital, analogue, photonics) focus. The selection of DETs should take place via an open and inclusive process, based on fulfilment of certain technical and security requirements. Any design service provider fulfilling such requirements may apply for integration into the platform. The PCT should provide the set of requirements that DETs must fulfil in order to apply for integration in the cloud-based platform.
To this end this work programme includes the following topics:

- Cloud platform for the European Design Platform
- Set-up and integration of Design Enablement Teams
- Support to start-ups and SMEs.
- Open-source EDA tools development
- Low power Edge AI Chips

[4] A foundry aggregator is an industry standard term used for companies that act as an intermediary between fabless semiconductor companies (clients) and semiconductor foundries (manufacturers). Typically, only large enterprises directly engage with foundries.

3.1.1 Cloud platform for the European Design Platform

Type of Action	Call for tenders
Indicative EU budget (from the DEP budget)	15 M€
Mode	EU funding only

Context

Note: A formal call for tenders will be published over the course of 2025. The current text should not be considered as a formal Call for Tenders within the context of a procurement procedure. Information listed here is purely indicative.

Chip design is a key weakness in Europe's semiconductor ecosystem. Fabless revenues in Europe represent less than 1% of global revenues. Recognising the importance of this sector to the value chain, Pillar 1 of the Chips Act, the Chips for Europe Initiative foresees a design platform to enable start-ups and SMEs to venture in design. The Design Platform is foreseen to serve as a hub of services and resources for its users and to this end the Chips Joint Undertaking should procure a cloud infrastructure to enable the implementation of said platform. The cloud infrastructure should include both the underlying cloud service as well as any related development of custom software.

Scope

The central cloud infrastructure should host the IP, PDKs and open-source EDA tools as well as training services. This should be accompanied by a user authentication service. Interested parties should therefore be responsible for the provisioning and management of a secure and scalable cloud infrastructure capable of hosting these key elements of the Design Platform and its associated services. The selected service provider should be responsible for the setting up and maintenance of this service for 4 years.

This should be accompanied by a vendor-neutral software solution for automated infrastructure configuration, referred to here as Infrastructure as Code (IaC), to be deployed at the various Design Enablement Teams as part of a federated cloud infrastructure for the Design Platform. The purpose of this IaC should be to:

- **Standardise deployment**: The IaC should enable the Platform Coordination Team (PCT) to define and enforce a standardised configuration for DET cloud environments through code, ensuring that all DETs adhere to the same security protocols, service level agreements, and access controls. This would ensure a more consistent and reliable user experience across different DETs.
- **Automate provisioning**: The IaC related tools should be used to automate the provisioning of cloud resources for DETs. This would simplify the process of setting

up and scaling design environments, reducing the potential for manual errors and freeing up DET resources to focus on user support and other value-added services.

- **Ensure version control and reproducibility**: Through the IaC, the PCT should be able to leverage version control systems to track changes and ensure that environments can be easily reproduced. This should be crucial for maintaining consistency over time, simplifying troubleshooting, and facilitating the rollback of changes if needed.
- **Enhance security and compliance**: The IaC can help enforce security best practices by automating security configurations and checks. This could be particularly relevant for the DP, given the sensitive nature of design data and IP. By codifying security policies, the PCT could help ensure a more secure and compliant design environment for all users.

Expected outcomes.

The requested cloud services should primarily contain the following elements:

- A repository populated with an extensive portfolio of open-source and proprietary 'design assets' to facilitate and enhance the design process for users, such as intellectual property (IP) blocks, design templates, fast adoption kits, process design kits (PDKs) from pilot lines and open foundries, open-source design tools, as well as reusable open-access design elements from previous EU-funded projects.

- Any suitable features, such as user authentication and license usage monitoring, that are deemed useful for the management of the overall initiative and the various DETs in the Design Platform.

- Templates of virtual machines or containers containing all the software components and configuration required to operate a given electronic design software, and that can be easily deployed on the cloud instances operated by the DETs.

The selected tender should also be responsible for the running and maintenance of this service for 4 years.

The latter point should be complemented by the development of an *Infrastructure as Code* (IaC) framework that supports a variety of cloud vendors. Work related to the development and management of the IaC should be coordinated by the PCT and deployed across various DETs. The purpose of this IaC is to facilitate cloud deployment at the various DETs, ensure baseline security standards, and provide a consistent experience across different DETs. Where possible, cloud vendor-agnostic resources should be used, accompanied by vendor-specific configurations where necessary. The service of developing the IaC should also be procured by the Chips JU with the technical assistance of the PCT.

All resources involved in this development should be based in the EU, including the location of the cloud-related data centres.

Further details will be presented in the Call for Tenders when published.

3.1.2 Set-up and integration of Design Enablement Teams

Topic: DIGITAL-JU-Chips-2025-CSA-DET

Type of Action	CSA
Indicative EU budget	5 M€
Expected EU contribution per project	The JU estimates that an EU contribution of around EUR 0.5 million would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	EU funding only One stage Call with submission of Full Proposal (FPP)
Call launch date	*04th of June 2025*
Deadline FPP Phase	*30th of July 2025*

Context

Semiconductor circuit design is the process of creating integrated circuits (ICs) by defining the functionalities and characteristics of chips, capturing a substantial portion of the added value within the semiconductor value chain. The trend is moving towards more complex, application-specific, highly integrated semiconductors, making cutting-edge design crucial for competitiveness and differentiation in a wide range of applications. In this context, fabless semiconductor companies are well-positioned to drive technological advancements and meet the needs of diverse applications, reinforcing their pivotal role and growth in the semiconductor industry.

The Chips Act underscores the strategic importance of fostering chip design growth in Europe to enhance the competitiveness of the Union’s semiconductor industry. Pillar I of the Chips Act, the Chips for Europe Initiative, outlines an ambitious plan to strengthen the Union's resilience in semiconductor technologies, including promoting the growth of fabless semiconductor companies. This is especially pertinent given that the European share of global fabless semiconductor companies’ revenues has shrunk to critically low levels, highlighting the urgent need for strategic initiatives to bolster this sector and enhance Europe's competitiveness. A critical mass of fabless companies is also key to generate further demand that would justify increased investment in semiconductor manufacturing capacity in Europe.

The Design Platform is at the heart of the Chips for Europe Initiative. It is envisaged as a key instrument for fostering the development of a strong semiconductor design ecosystem in the Union, by supporting the growth of highly innovative European fabless start-ups and SMEs. Considering the Union’s limited fabless capacity, and the significant barriers to entry

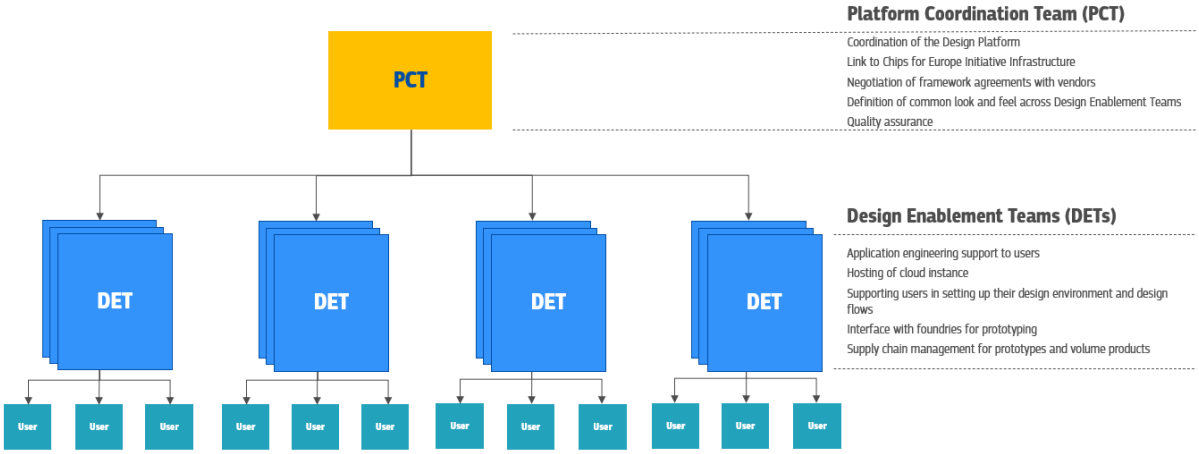
in chip design, the Design Platform will focus on nurturing emerging companies in the sector by enabling their access to a comprehensive chip design ecosystem from early stages up to tape-out.

This ecosystem includes a series of Electronic Design Automation (EDA) tools, Intellectual Property (IP) blocks and Process/Assembly Design Kits (P/ADKs) including standard cell libraries. This is coupled with either on-premise or cloud-based computing resources. Furthermore, access to foundries, packaging and test facilities is crucial. Each of these elements requires a separate acquisition process for the designer, often involving very significant costs and its own complex procedures.

Scope

The Design Platform should act as a hub of services to support European companies engaged in chip design. The Design Platform is implemented via two main classes of entities:

- The **Platform Coordination Team (PCT)** which coordinates the Design Platform, establishes framework agreements with EDA/IP suppliers and provides access to a central cloud service encompassing a marketplace with open source or proprietary IPs/EDA tools/PDKs and trainings amongst other resources. The PCT also provides DETs with Infrastructure as Code to ease the deployment of cloud instances. Through internal expertise and, where necessary, sub-contracting, the PCT and DETs collaborate to design and implement the overarching technical implementation of the platform and design interfaces with the distributed services, as well as ensuring the overall neutrality of the platform
- The **Design Enablement Teams (DETs)** each of which is in charge managing a distributed cloud instance and providing dedicated application engineering support to users from setting up their design environment and design flows up to tape-out. A DET can be a single entity, or a consortium of entities selected among providers of chips design support services, such as design houses, RTOs or other entities currently providing design enablement services on a commercial basis. DETs should be selected based on their technology expertise (e.g., digital, analogue, mixed-signal, photonics, etc.), ability to offer support across the end-to-end design flow, access to fabrication services (foundries, packaging, test services) and a proven track record of delivering high quality services to users, amongst other characteristics.



A call (*DIGITAL-Chips-2024-CSA-CDP-1*) to select a Platform Coordination Team was launched in July 2024. The scope of the current call is to select a number of Design Enablement Teams.

Expected outcomes.

The core functions of DETs include, but are not limited to:

1. **Deployment of Electronic Design Automation (EDA) tools on the cloud**: DETs will manage secured cloud instances facilitating access to essential design tools and simulation environments. To this end, DETs may contract with a cloud provider of their choice to setup this infrastructure.[5] It is expected that prospective DETs demonstrate experience in commercial designs using tools from established EDA vendors.
2. **Design flow support and customisation**: DETs will assist users in setting up and customising design environments and flows, ensuring smooth progression from initial setup to tape-out.
3. **Application engineering**: DETs will offer dedicated application engineering support, addressing specific user needs and challenges throughout the development process.
4. **Access to Process Design Kits (PDKs)**: DETs will provide users with access to the necessary PDKs and ADKs for their design projects. Each DET must have legal authorisation to use and/or provide its users access to PDKs/ADKs of at least one semiconductor foundry.
5. **Design expertise**: DETs will provide users with access to the necessary design expertise for their design projects, directly via the DET's resources and/or through partnerships with third parties.
6. **Prototyping and fabrication services**: DETs will facilitate prototyping and fabrication services including packaging and testing through partnerships with leading foundries

[5] Cloud services utilised by the DET shall comply with robust cybersecurity security requirements such as the CEN/TS 18026:2024 standard or equivalent.

or aggregators, the Chips for Europe Initiative pilot lines or other relevant pilot lines. Each DET must have already established direct or indirect relationships with at least one semiconductor foundry, enabling efficient communication and ensuring technology advice and support to its users.

Overall, it is expected that each DET should manage a cloud instance offering dedicated application engineering support to users, from setting up their design environment and design flows to tape-out. The level of security of that cloud instance should be commensurate to the categories of users and applications that are expected to be running on this instance. The DET will maintain a cloud-based connection to the PCT's central cloud to manage user access, extend its capacity with additional resources (open-source IPs, EDA Tools, PDK...) and deliver periodic monitoring data to increase the quality of service of the Design Platform.

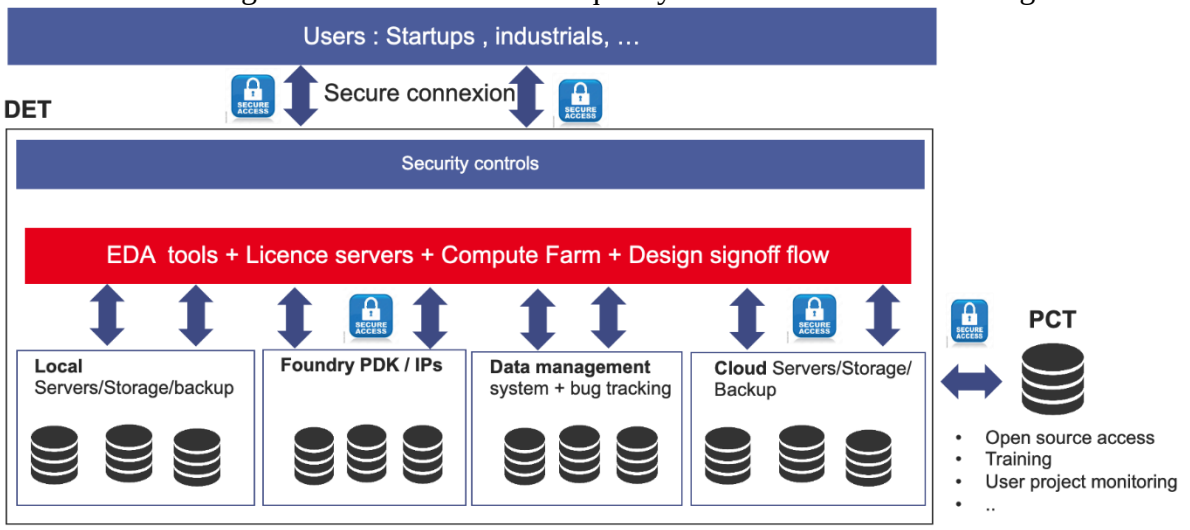


Figure 2 - High-level illustration of DET cloud-instance

DETs will be selected based on the extent of their technology expertise (e.g. digital, analogue, mixed-signal, photonics, etc.), ability to offer support across the end-to-end design flow, including PPA optimisation, access to fabrication services, and a proven track record of delivering high-quality services to users, among other characteristics.

These DETs could be public or private organisations that offer custom design support services, such as ASIC design houses and RTOs, with a demonstrated track record of expertise and experience in providing such services. Overall, the DETs should cover a wide variety of semiconductor technologies and can have different sectoral focuses (e.g. automotive, defence).

The only eligible costs for beneficiaries are those **directly related to the set-up and integration of DET's cloud services into the design platform**. This integration will be executed through a shared customer portal and the deployment of an Infrastructure as Code solution developed specifically for the Design Platform to ensure a consistent user experience. The PCT will give access to these solutions to the designated DETs, for instance through an API. Any costs related to the infrastructure of the cloud provider of choice or through on-

premise infrastructure, are considered to be part of the standard business proposition and competitive offering of the DET; as such, these costs are not considered eligible.

During the initial phase, the central cloud infrastructure of the design platform is likely to be still under development and thus not yet available for integration with the DET cloud service. Nevertheless, a preliminary trial phase of the design platform involving a limited set of test users may commence, and the selected DETs should be prepared to provide support and enablement services directly to such users from their own infrastructure, until the central platform becomes available for full service integration.

The selection process will ensure that collectively the selected DETs cover a broad range of technologies (CMOS and more than Moore technologies) and design topologies (analog, digital, mixed-signal etc.), for various applications (e.g. automotive, aeronautics, consumer, health etc). Preference will be given to DET candidates that address in their proposal at least one of the following technologies: CMOS bulk, FDSOI, finFET or Photonics. Strategies to collaborate with the Chips for Europe Initiative pilot lines are highly valued.

Proposals should provide a detailed explanation of the cloud services to be used by the DET, including their performance specifications and cybersecurity measures. Cloud services utilised by the DET should comply with robust cybersecurity requirements.[6]

DETs should also demonstrate capacity to effectively serve users across all the participating states of the Chips JU.

Finally, DET proposals which include members of the PCT consortium should clearly demonstrate effective measures to establish and maintain a strict separation between the two entities, including separate personnel and controlled communication channels, in order to ensure the full neutrality and independence of the PCT.

Admissibility

Admissibility conditions are described in Annex 2 “General DIGITAL EUROPE PROGRAMME conditions” of the WP General Annexes.

Regarding page limits:

- The page limit for the chapter RELEVANCE is 10 pages.
- The page limit for the chapter IMPLEMENTATION + chapter 4 of the template for the proposal (Part B) is 40 pages.
- The page limit for the chapter IMPACT is 10 pages.

Eligibility

Eligibility conditions are described in Annex 2 of the WP General Annexes.

[6] Such as the CEN/TS 18026:2024 standard or equivalent.

The following exceptions apply:

- Subject to participation restrictions for the protection of European digital infrastructures, communication and information systems, and related supply chains, as described in Annex 4 of the WP General Annexes.
- Legal entities that are established in the Union or EEA countries but are controlled from third countries may only participate on the condition that they guarantee the protection of the essential security interests of the Union and the Member States and that they ensure the protection of classified documents information. Where applicable, security guarantees need to be provided after proposal selection.

Financial and operational capacity and exclusion

Please refer to Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).
For the priority order of proposals with the same score, please refer to Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Award criteria.

Please refer to Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Specific rules may apply regarding the eligibility to national funding.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Scores

The scores will be given with a resolution of one decimal.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Relevance	0-5	1	3
Implementation	0-5	1	3
Impact	0-5	1	3
Total	0-15		10

(*) threshold applies to unweighted score.
(**) the weight is only used to establish the ranking of the proposals.

Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to DIGITAL.

Type of beneficiary	**Maximum EU Contribution as % of eligible costs according to DIGITAL**
For profit organization but not an SME	100%
SME (for profit SME)	100 %
University/Other (not for profit)	100 %

3.1.3 Support for start-ups and SMEs

Topic: HORIZON-JU-Chips-2025-IA-SUP

Support to start-ups and SMEs making use of the Design Platform

Specific conditions	
Type of Action	Grant to identified beneficiary according to Financial Regulation Article 198 (f) – Innovation Action
Indicative EU budget	EUR 220 million.
Legal and financial set-up of the Grant Agreements	The rules are described in General Annex G of Horizon Europe Work Programme 2025[7]. The following exceptions apply: Beneficiaries may provide financial support to third parties. The support to third parties can only be provided in the form of grants. The EUR 60 000 threshold provided for in Article 207(a) of the Financial Regulation No 2024/2509 does not apply in order to be able to achieve the objectives of this action. The maximum amount of FSTP to be granted to an individual third party is EUR 8.1 million.
Mode	One stage, with submission of Full Project Proposal (FPP) FSTP recipients co-funded with NFA
Invitation date	03 December 2025
Deadline FPP	14 January 2026

3.1.3.1 Context

The Chips Act underscores the strategic importance of fostering the growth of chip design activities in Europe to enhance the competitiveness of the Union's semiconductor industry. Pillar I of the Chips Act, the Chips for Europe Initiative, outlines an ambitious plan to strengthen the Union's resilience in semiconductor technologies, also by promoting the growth of fabless startups. These fabless startups are key drivers of innovation, playing a crucial role in key sectors such as AI, telecommunications, and automotive.

[7] https://ec.europa.eu/info/funding-tenders/opportunities/docs/2021-2027/horizon/wp-call/2025/wp-14-general-annexes_horizon-2025_en.pdf

As fabless companies continue to drive growth in the semiconductor industry, the European share of global fabless semiconductor companies' revenues has shrunk to critically low levels. This highlights the urgent need for strategic initiatives to bolster this sector and enhance Europe's competitiveness. A critical mass of fabless companies is also key to generate further demand that would justify increased investment in semiconductor manufacturing capacity in Europe.

Currently, fabless start-ups can already find support in initiatives such as the Chips Fund, the Strategic Technologies for Europe Platform (STEP) programme, competence centres, and pilot lines. However, there is a crucial gap at the very early stages of these companies which the Design Platform seeks to address.

The Design Platform is at the heart of the Chips for Europe Initiative. It is a key instrument to foster the development of a strong design ecosystem in the Union by creating a pipeline of highly innovative European fabless companies. A key goal of the Design Platform is to support the growth of fabless companies by providing access to funding, foundries, design tools, IP and computing resources.

A consortium to manage the Design Platform, referred to as the Platform Coordination Team (PCT) was selected following a Call for Expression of Interest in Appendix 4 of the Chips Joint Undertaking Multiannual Work Programme 2023-2027. The same consortium was selected following a Call for Proposals for a Coordination and Support Action under Digital Europe in the aforementioned work programme. To ensure the overall coherence of the Platform, to give users a single point of contact, and considering its technical expertise, the consortium is expected to manage a start-up and SME support programme for early stage companies.

This action aims to add a particular aspect to the aforementioned support programme, the disbursement of grants, as well as potentially additional acceleration, incubation and other support activities catered to selected FSTP recipients.

Scope

Amongst others, the beneficiaries will be responsible for organising and implementing FSTP calls and their evaluations, administering the disbursement of grants and for additional support activities.

This programme will address a key gap in the support of early-stage start-ups and SMEs prior to commercialisation of their innovation. Supported third parties are expected to present innovative chip design projects with a clear perspective towards commercialisation. The programme will facilitate the scaling up of start-ups and SMEs engaged in chip design through FSTP grants.

The beneficiaries will collaborate with the providers of incubation and acceleration services that are funded via a Digital Europe grant for a Coordination and Support Action. The supported third parties will benefit from FSTP grants as well as incubation and acceleration services. In addition, the beneficiaries of this topic will work together with Design Enablement

Teams, who will provide dedicated application engineering support to users from setting up their design environment and design flows up to tape-outs.

Selections and Evaluation procedure to be run by the beneficiaries

Selections should be made by the beneficiaries with the assistance of a pool of independent experts that evaluate the proposals. Experts should be professionals from the field of semiconductor design or manufacturing and should have an understanding of both the technology and the semiconductor industry.

The criteria for giving the financial support for FSTP Level 1 must include the capacity of the applying third party to realise a proof-of-concept design, level of innovation, and EU added value. Beneficiaries are expected to further elaborate on these criteria.

The criteria for giving the financial support for FSTP Level 2 must include the quality of the business case, market viability of possible final products, the quality of the proof-of-concept demonstrator and designs, level of innovation, and EU added value. Beneficiaries are expected to further elaborate on these criteria.

The beneficiaries should establish a quick selection procedure to verify the eligibility of the third party and the capacity of the applying third party to realise a proof-of-concept design or a proof-of-concept demonstrator.

Scope for FSTP Level 1

The following applies to the selection of third parties receiving Level 1 services:

- Third parties should be invited to submit proposals for Level 1 services via a continuous application process with a number of cut-off dates determined by the consortium. There should be at least 2 cut-off dates per year during the continuous application period.
- Selected third parties must design the majority of their chips in-house, in the country of establishment.
- The maximum amount of financial support for Level 1 services should not exceed EUR 100 000 for each third party. A third party may only benefit from Level 1 services once; this includes linked entities.
- The exact amount of the financial support is based on estimates of the eligible costs given by the applicant and assessed by experts designated by the PCT. The funding rate will be up to 100%. Funding may be awarded in the form of lump sums. Funding is paid out based on reaching well-defined milestones. Prefinancing may be awarded as well.

Financial support for FSTP Level 1

Via FSTP calls, selected startups and SMEs may receive a grant covering certain pre-determined eligible costs.

- The financial support is granted to cover:

- Electronic Design Automation (EDA) tool license costs with vendors that have a "General Conditions Agreement" within the context of the Design Platform;
- semiconductor Intellectual Property (IP) blocks licence costs;
- DET services costs and/or costs related to access to computing resources;

Scope for FSTP Level 2

The following applies to the selection of third parties receiving Level 2 services:

- Third parties are invited to submit proposals for Level 2 services via a continuous application process with a number of cut-off dates determined by the consortium.[8] There should be at least 2 cut-off dates per year during the continuous application period.
- Selected third parties must design the majority of their chips in-house, in the country of establishment.
- The maximum amount of financial support for Level 2 services should not exceed EUR 8 000 000 for each third party. A third party may only benefit from Level 2 services once; this includes linked entities.
- The exact amount of the financial support is based on estimates of the eligible costs given by the applicant and assessed by experts designated by the PCT. The funding rate will be up to 35% Union funding, and may be complemented up to 70% by national and/or Union funding. Funding may be awarded in the form of lump sums. Funding is paid out based on reaching well-defined milestones. Prefinancing may be awarded as well.

Financial support for FSTP Level 2

Via FSTP calls, selected startups and SMEs may receive a grant covering certain pre-determined eligible costs.

Start-ups and SMEs in Level 2 may benefit from two main funding streams, provided from the Union's contribution and the Participating States' contribution.

- The financial support is granted to cover:
    - Electronic Design Automation (EDA) tool license costs with vendors that have a "General Conditions Agreement" within the context of the Design Platform;
    - semiconductor Intellectual Property (IP) blocks licence costs;
    - DET services costs and/or costs related to access to computing resources;
    - fabrication costs for prototyping.

[8] Prior use of Level 1 services is not a prerequisite for eligibility to apply for Level 2 services.

Admissibility for applications for FSTP

- Third parties should submit applications in a format defined by the PCT consortium. The complexity and length of the applications should be proportionate to the size of the grant.
- Proposals by third parties responding to FSTP calls should include:
    - a description and justification by the third party of the proposed costs;
    - evidence of the third party's financial capacity to carry out the proposed project, considering that a certain part of overall costs may need to be financed by the third party;
    - a description of the project as well as the professional experience of the third party;

Eligibility for start-ups and SMEs applying for FSTP

All organisations that are eligible for funding in Horizon Europe are eligible for funding in the FSTP calls organised by the beneficiaries. Recipients of FSTP grants will be granted access to the Design Platform[9].

For further conditions on financial support to third parties, proposers are referred to the Horizon Europe General Annexes[10].

In addition to eligibility to participate, for the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Expected outcomes.

A main element of the Design Platform is a **start-up and SME incubation and acceleration programme** that is broadly based on two levels of support as seen in Figure 1.

This programme relies on the cloud service infrastructure managed by the PCT and procured by the Chips Joint Undertaking, as well as services provided by both the PCT and the Design Enablement Teams (DETs) following calls DIGITAL-Chips-2024-CSA-CDP-1 and DIGITAL-JU-Chips-2025-CSA-DET respectively.[11]

Within the context of this action, Level 1 services correspond to an incubation programme and Level 2 services correspond to an acceleration programme.

[9] It should be noted that previous work programmes (in particular, Annex 4 of the Chips JU's multi-annual work programme) provided other statements about access to the Design Platform. This has been corrected in the current work programme and in the access conditions specified in the Hosting Agreement, i.e., the formal agreement between the PCT consortium and the Chips JU that defines how the Design Platform is to be managed. It is therefore necessary to clarify here that recipients of FSTP grants will have access to the Design Platform and that all organisations eligible for Horizon Europe funding are also eligible for financial support under the FSTP calls of this topic.

[10] https://ec.europa.eu/info/funding-tenders/opportunities/docs/2021-2027/horizon/wp-call/2025/wp-14-general-annexes_horizon-2025_en.pdf

[11] As set out in Annexes 4 and 6 of the Chips Joint Undertaking's multi-annual work programme 2023-2027

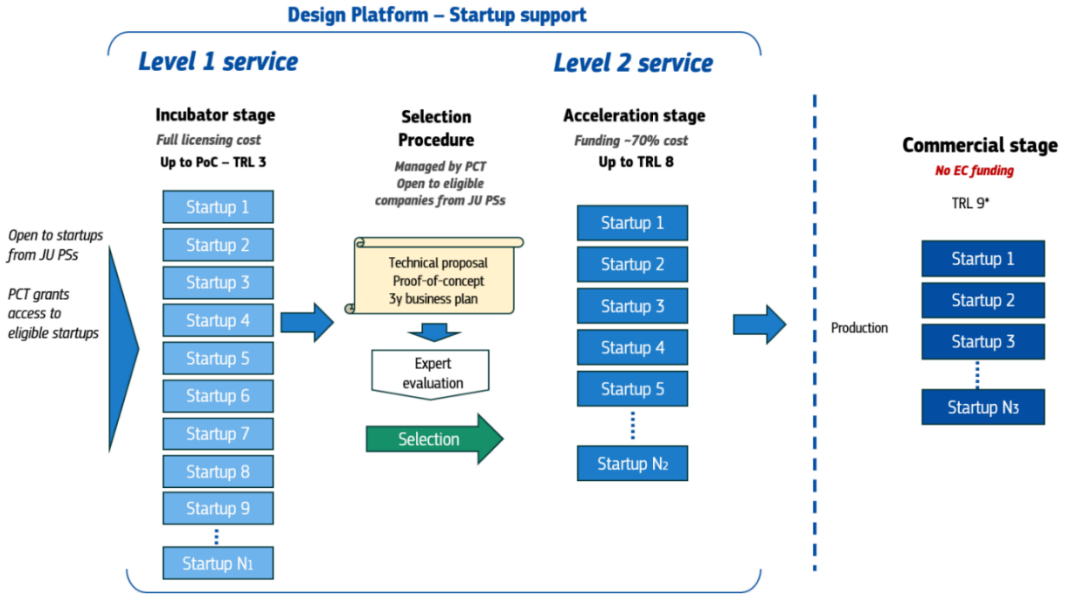


Figure 1 – Design Platform start-up and SME support programme

Beneficiaries need to ensure that Level 1 support is widely promoted and accessible to fabless European start-ups and SMEs. Here users will be given access to *proof-of-concept* licenses, IP and services that are usually subject to nominal fees. These fees will be partly financed via this action through grants to third parties. Level 1 support is primarily aimed at spinouts and early-stage start-ups.

Start-ups and SMEs at a more advanced stage of development may apply to a selection process to qualify for the Level 2 programme, which offers funding to cover up to 70% of the eligible costs for the selected companies. It is expected that the EU contribution provided via the PCT consortium plus national funding will cover up to 70% of eligible costs. It is expected that in the typical case the JU funding rate is up to 35%. The FSTP calls, including EU funding rates, should be discussed with the Chips JU before the opening of new and revised FSTP calls[12]. Here, EDA and IP license costs and/or conditions should be subject to a "General Conditions Agreement" or MoU agreed to by the Chips Joint Undertaking and made available to the Platform Coordination Team for users of the Design Platform.

Beneficiaries should ensure effective coordination with services and support activities for start-ups and SMEs financed by the Union outside of this action, particularly through the Coordination and Support Action (CSA) grant awarded to the DECIDE consortium acting as the Platform Coordination Team[13], to ensure that FSTP grantees are systematically monitored and supported.

[12] For administrative purposes, the maximum EU funding rate is considered to be 100%.
[13] Following a Call for Proposals in Annex 4 of the Chips Joint Undertaking's multi-annual work programme 2023-2027

The beneficiaries should demonstrate in their proposal the capacity to effectively organise and implement FSTP calls and their evaluations, to disburse grants to startups and SMEs, to assess performance of FSTP recipients, and to track progress over time.

Out of the total amount of EUR 220 million EU funding, the consortium is expected to commit at least 98% on financial support to third parties. At most 2% should be reserved to organise, evaluate, and manage FSTP calls, including awarding and monitoring and reviewing the execution of activities of FSTP recipients, and to execute other support activities. Incubation and acceleration services in addition to those funded via the Digital Europe grant for a Coordination and Support Action (CSA)[14] may be covered as well, if duly justified. Other activities, where deemed necessary for achieving the objectives of the topic, may be proposed as well. Support activities proposed need to be clearly delineated from those covered elsewhere.

Concretely, the following outcomes are expected:

- an effective and efficient start-up and SME support programme;
- a pipeline of sustainable fabless companies that have gone through an acceleration phase.

Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Regarding page limits:

Chapter	**FPP Phase**
Excellence	60 pages
Impact	100 pages
Quality and efficiency of the Implementation	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

[14] DIGITAL-Chips-2024-CSA-CDP-1 in Annex 4 of the Chips Joint Undertaking's multi-annual work programme 2023-2027

Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions (JU Grant):

Use of Article 198(f) of the Financial Regulation

Pursuant to Article 198(f) of the Financial Regulation, a grant may be awarded without a call for proposals for activities with specific characteristics that require a particular type of body on account of its technical competence, high degree of specialisation, or administrative powers, provided that the activities concerned do not fall within the scope of a call for proposals.

The DECIDE consortium acting as the Platform Coordination Team (PCT) and Hosting Consortium of the Design Platform following:

- a Call for Expression of Interest and a Digital Europe Call for Proposals in Appendix 4 of the Chips Joint Undertaking multiannual work programme 2023-2027 (REF: Chips-2024-CDP);
- evaluations by the Chips Joint Undertaking with the support of independent, suitably qualified experts; and
- selection and funding decisions by the Public Authorities Board of the Chips Joint Undertaking on the basis of a ranking list provided by independent experts;[15]

is deemed as the appropriate body to pursue this action in line with Article 198(f) of the Financial Regulation by fulfilling all the conditions required for the application of this provision, as set out below:

- The selected PCT consortium, *DECIDE*, is responsible for operating and coordinating all aspects of the Design Platform. This includes user onboarding and support, operation of the central cloud infrastructure, coordination of related design enablement services, and the implementation of mentoring, incubation, and acceleration programmes for start-ups and SMEs.
- Financial support to selected third parties, particularly start-ups and SMEs, making use of the Design Platform, as envisaged in this action, is a core feature of the Design Platform. Financial support for access to tools, IP, design enablement services and access to prototyping services is key to ensure that third parties can exploit the benefits provided by the deployed infrastructure.
- Annex C of the work programme[16] explicitly mandates that the selected "*PCT consortium shall be in charge of running a start-up incubation programme and a start-up acceleration programme in collaboration with the selected DETs*". Furthermore, the action corresponds to Phase 4 of the Design Platform's development, as outlined in

[15] Decision PAB 2024.56
[16] Appendix 4 Chips Joint Undertaking Multiannual Work Programme 2023-2027

Section 4.1.3 of the call for proposals REF Chips-2024-CDP-1,[17] under which the PCT consortium was selected. Section 4.1.3.2 of the call text explicitly makes clear that this phase involves providing support to start-ups and SMEs, complemented by contributions from Participating States.

- Due to the integrated nature of the Platform, this action requires tight coupling with the already ongoing activities of the PCT, financed through Chips-2024-CDP-1. Indeed, this action demands intricate knowledge of the Platform's architecture and user base, the ability to manage sensitive contractual arrangements with Electronic Design Automation (EDA) tool vendors negotiated by the PCT, and needs to be tightly coupled with the delivery of tailored support services to start-ups and SMEs. Via the PCT, start-ups and SMEs will have a single-point-of-contact for all services and support stemming from the Design Platform. Therefore, it would be inefficient for such activities to be executed by an entity independent of the PCT consortium.
- In addition, the DECIDE consortium will run a mentoring programme and already has the technical and organisational capacity to implement acceleration and incubation activities. Therefore, given that the DECIDE consortium is already funded via a grant to implement acceleration and incubation activities for all startups and SMEs, it is best placed to manage the complementary financial support to third parties participating in incubation and acceleration activities, as well as potentially additional acceleration, incubation and other support activities catered to selected FSTP recipients.

Furthermore, the activities covered by this invitation to submit a proposal represent a direct complement of work already entrusted to the PCT through a competitive procedure. This action is essential to the ongoing development and stability of the Design Platform. It is in line with Article 198(f) of the Financial Regulation and it is not within the scope of a call for proposals.

The PCT consortium is composed of the following legal entities:

1. INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM (IMEC), PIC 999981149, established in KAPELDREEF 75, LEUVEN 3001, Belgium, acting as the coordinator;
2. COMMISSARIAT A L'ENERGIE ATOMIQUE ET AUX ENERGIES ALTERNATIVES(CEA), PIC 999992401, established in RUE LEBLANC 25, PARIS 15 75015, France;
3. FRAUNHOFER GESELLSCHAFT ZUR FORDERUNG DER ANGEWANDTENFORSCHUNG EV (FHG), PIC 999984059, established in HANSASTRASSE 27C, MUNCHEN80686, Germany;
4. IHP GMBH - LEIBNIZ INSTITUTE FOR HIGH PERFORMANCEMICROELECTRONICS (IHP), PIC 999606438, established in IM TECHNOLOGIEPARK 25,FRANKFURT ODER 15236, Germany;
5. SILICON AUSTRIA LABS GMBH (SAL), PIC 901837907, established in SANDGASSE 34,GRAZ 8010, Austria;

[17] *Idem*

6. CENTRO ITALIANO PER IL DESIGN DEI CIRCUITI INTEGRATI ASEMICONDUTTORE (CHIPS-IT), PIC 878999548, established in VIA SANT'ENNODIO 26,PAVIA 27100, Italy;
7. AGENCIA ESTATAL CONSEJO SUPERIOR DE INVESTIGACIONES CIENTIFICAS(CSIC), PIC 999991722, established in CALLE SERRANO 117, MADRID 28006, Spain;
8. INTERNATIONAL IBERIAN NANOTECHNOLOGY LABORATORY (INL), PIC988145985, established in AVENIDA MESTRE JOSE VEIGA, BRAGA 4715-330, Portugal;
9. TECHNISCHE UNIVERSITEIT EINDHOVEN (TU/e), PIC 999977269, established in GROENE LOPER 3, EINDHOVEN 5612 AE, Netherlands;
10. TAMPEREEN KORKEAKOULUSAATIO SR (TAU), PIC 902999288, established in KALEVANTIE 4, TAMPERE 33100, Finland;
11. 11. CESKE VYSOKE UCENI TECHNICKE V PRAZE (CVUT), PIC 999848744, established in JUGOSLAVSKYCH PARTYZANU 1580/3, PRAHA 160 00, Czechia;
12. AKADEMIA GORNICZO-HUTNICZA IM. STANISLAWA STASZICA W KRAKOWIE(AGH), PIC 999844573, established in AL ADAMA MICKIEWICZA 30, KRAKOW 30-059, Poland;

A sub-set of the PCT consortium with selected legal entities from the ones above-mentioned may also be eligible for this call.

Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU.[18]

Award criteria

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU. [19]

[18] Decision GB 2024.71
[19] *Idem*

Scores

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Relevance	0-5	1.0	3
Implementation	0-5	1.0	3
Impact	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

This is not related to anything. There are no such % in the FSTP or in the SUP

Reimbursement rate for establishing the EU contribution

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	Maximum EU Contribution as % of the Eligible Cost according to HE (*)
For profit organization but not an SME	70 %
SME (for profit SME)	70 %
University/Other (not for profit)	100 %

(*) beneficiaries may ask for a lower contribution.

On the maximum amount of financial support in line with Article 207(a) of the Financial Regulation

To achieve the objectives of this action, namely to provide start-ups and SMEs access to foundries, design tools, IP and computing resources, in line with the aims set out by the Chips Act, the maximum amount of financial support that can be paid to a third party must exceed the EUR 60.000 threshold set out in Article 207(a) of the Financial Regulation.

The nature of the costs related to the provision of Electronic Design Automation (EDA) tool licenses, IP licenses, foundry costs, computing resources and design enablement services, inherently surpass the threshold. As such, the objective of this action would be impossible to achieve without exceeding it.

Therefore, in accordance with paragraph 3 of Article 207(a) the threshold is exceeded and set at EUR 8.100.000.

3.1.4 Open-source EDA tools development

Topic: HORIZON-JU-Chips-2025-IA-EDA

Type of Action	Innovation Action (IA)
Indicative EU budget	20 M€
Expected EU contribution per project	The Chips JU estimates that an EU contribution of between EUR 6 and 7 million per project would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Two stage Call, with submission of Project Outline (PO) and Full Project Proposal (FPP)
Call launch date	04 March 2025
Deadline PO	29 Apr 2025 at 17:00 Brussels Time
Deadline FPP Phase	17 Sep 2025 at 17:00 Brussels Time

Context

A key objective of the Chips Act under the Chips for Europe Initiative is the 'building up of advanced design capacity for integrated semiconductor technologies'. To this end as part of operational objective 1 of the Chips Act, the Initiative should integrate 'new design facilities with extended libraries and electronic design automation (EDA) tools' into a virtual design platform. As part of a broader suite of resources, the Design Platform will make available a number of open-source tools.

Chip design is a vital element in the semiconductor value chain and open-source Electronic Design Automation (EDA) tools can be key drivers for innovation in this sector by enabling researchers and developers to experiment with new algorithms, architectures, and methodologies.

Access to EDA software, essential for chip development, has traditionally been both heavily restricted and prohibitively expensive, creating significant barriers for start-ups and small-to-medium-sized enterprises (SMEs). Open-source EDA tools can empower start-ups and SMEs with cost-efficient alternatives to expensive commercial licenses, allowing SMEs to

experiment with chip design. This is particularly crucial for SMEs operating in low- to mid-volume production.

Moreover, Europe is facing a considerable workforce shortage in this sector. This requires the cultivation of an open ecosystem to attract and develop more designers and developers. Open-source EDA tools lower the barrier of entry to chip design and thus attract new engineers and chip designers. Students and new entrants in the field can experiment with chip design without limitations on exploitation of their design or restrictive non-disclosure agreements (NDAs), fostering learning and experimentation. Therefore, wide-spread dissemination of these tools can help in addressing the skills gap in the semiconductor industry.

Existing open-source toolchains already support complete chip designs in several mature nodes, which are the technology of choice in a number of applications in fields such as radar design, automotive, aeronautics and space, medical technology, and electronics for harsh environments—industries with a strong European market presence. With relatively low tape-out costs, these nodes present minimal barriers for SMEs, and open-source tools could enable a wide array of European companies and start-ups to enter the chip design arena.

The growing accessibility of low-cost computing resources has opened the door for large-scale exploitation of parallel computing in EDA. However, this potential is often constrained by licensing costs, which limit the number of parallel runs needed for comprehensive adoption. This is an area where open-source implementations can be an interesting proposition. The ability to fully leverage computational resources for unrestricted parallel scaling—especially with the integration of modern machine learning technologies—has become a focal point of interest for many organisations seeking to push the boundaries of innovation.

Therefore, it is expected that over time, open-source EDA tools will offer significant benefits across other areas of chip design, including advanced nodes and highly integrated digital circuits, fostering growth and enhancing efficiency across the entire electronics sector.

The Horizon Europe *Go-IT* project[20] and the FOSSI Foundation have developed a roadmap for open-source hardware. This roadmap should be considered in proposals answering to this call.[21]

Proposals should, where relevant, build upon existing open-source resources and focus on advancing these tools to the next level. Efforts should include bridging the gap between open-source and commercial EDA tools - proposals should include a realistic outline with expectations and objectives to achieve this goal. Overall, proposals should include effective strategies for enhancing existing tools and improve user experience while driving innovation by introducing novel tools and methodologies. Where appropriate, machine learning techniques to improve performance and productivity should be considered.

[20] Go IT! | GOIT | Project | Fact sheet | HORIZON | CORDIS | European Commission
[21] Roadmap and Recommendations for Open Source EDA in Europe

Technology Readiness Level: Targeted TRL at the end of projects is between 7 and 8.

Scope

Each proposal must address only one of the following three streams: (i) digital SoC design; (ii) analogue and mixed-signal design; or (iii) productivity, interoperability, and verification. Only one project per stream will be selected.

(i) Digital SoC design

Modern integrated circuit (IC) design thrives on digital workflows and advanced design automation tools, enabling engineers to capitalise on the increasing circuit density achieved with each new technology node. The exponential progress driven by Moore's Law not only fuels innovation at the industry's forefront but also broadens accessibility across the technological landscape, including at more mature nodes. While much attention is given to cutting-edge design nodes, the enhanced productivity these advancements bring also empowers SMEs, even those with limited design expertise, to undertake projects previously beyond their reach. This democratisation of IC design opens up new markets, fosters innovation, and drives growth across the sector.

Digital chip design serves as the backbone for developing processors, memory, and logic components that power a vast array of electronic devices—from smartphones and computers to IoT systems and cutting-edge AI hardware. Currently, open-source EDA tools for digital design provide sufficient support for mature technology nodes. However, advancing to more sophisticated nodes requires refining existing tools and expanding their functionality. As technology nodes become smaller, the impact of parasitic effects on overall performance—both in terms of power and timing—grows significantly. Continued development is essential to accurately model and mitigate these effects.

(ii) Analogue and mixed-signal design

For stable, mature nodes, the availability of open-source Process Design Kits (PDKs) and comprehensive open-source design flows already provides significant opportunities for analogue and mixed-signal integrated circuit (IC) design. These tools are particularly valuable for education and training, enabling students, researchers, and engineers to gain hands-on experience in designing, manufacturing, and testing custom analogue and mixed-signal chips. By lowering the cost and accessibility barriers, these resources play a crucial role in equipping the next generation of designers with practical skills, particularly in fields such as sensors, communication systems, and signal processing.

Looking to the short-to-medium term, the goal is to achieve performance and reliability on par with proprietary tools while expanding the capabilities of open-source EDA solutions. Specific focus will be given to advancing tools and methodologies for complex analogue, radio frequency (RF), and terahertz (THz) designs, as these are essential for emerging technologies such as IoT, 5G/6G, and advanced communication systems. By prioritising analogue and

mixed-signal functionality from the outset, open-source EDA tools can drive innovation and expand access for this key segment of Europe's semiconductor ecosystem.

(iii) Productivity, interoperability, and verification

Addressing the challenge of labour shortages requires targeted measures to enhance efficiency and accessibility in chip design. In the short term, further developing and leveraging open-source tools can significantly boost productivity by reducing barriers to entry for engineers and designers.

In the short-to-medium term, focusing on improving interoperability between various Electronic Design Automation (EDA) tools will be crucial. Seamlessly integrating open-source EDA tools into established design workflows will enable smoother collaboration between diverse teams and disciplines. This interoperability will reduce time-consuming inefficiencies caused by incompatible systems, streamlining the design process from conceptualisation to final tape-out. For SMEs, in particular, this integration will lower technical barriers, making advanced chip design more accessible and cost-effective.

Furthermore, investing in open-source design verification tools will deliver benefits to the entire chip design industry. Fast and efficient verification solutions with minimal access barriers are essential for accelerating time-to-market and fostering wider adoption. In the medium term, the development of innovative verification methodologies will further enhance efficiency, streamline design processes, and attract skilled talent from diverse disciplines, addressing the industry's growing demand for expertise.

Such advancements will not only address immediate labour shortages but also strengthen the productivity of European SMEs in key industries, supporting their innovation in a rapidly evolving global market.

Expected outcomes.

Results stemming from this call should be well documented and widely disseminated. Precise documentation, user manuals as well as video tutorials should be made available. Selected consortia must develop teaching materials and courses with open resources and examples based on the developed/improved open-source EDA tools, accessible to academic institutions across the EU and suitable for self-study by individuals. To this end, collaboration with initiatives such as EUROPRACTICE is encouraged.

Consortia should actively engage with the Platform Coordination Team of the Chips Act's Design Platform to integrate their tools into the platform's design flows. Proposals must outline a clear strategy for engaging with relevant foundries to secure access to the required PDKs.

Proposals should clearly specify the applicable OSI-approved open-source license for all results. Proposals should also include a sustainability plan for results following the end of the project.[22]

[22] https://opensource.org/licenses

The three selected consortia should collaborate in their technical work where relevant. Joint communication and dissemination efforts are encouraged.

The expected outcomes for each of the aforementioned streams are the following:

(i) Digital SoC design

The overall ambition of this stream is to ensure a comprehensive and stable digital design flow in more mainstream nodes (65-28nm). Improvement of tools in more mature nodes is also within scope of this stream. To this end a baseline for the quality of results currently achievable with current state-of-the-art open-source tools needs to be determined.

The following outcomes should be considered:

- **Improved open-source EDA tools**: Achieved better result quality and performance of existing open-source EDA tools, especially for large-scale designs.
- **Optimised parasitic extraction workflow**: Delivered enhanced accuracy and efficiency in parasitic extraction, validated through experimental results on fabricated integrated circuits (ICs).
- **Industry-standard memory generators**: Developed high-quality memory generators for both mature and advanced technology nodes, meeting industry requirements.
- **Enhanced hierarchical design flows**: Strengthened support for hierarchical design methodologies and incremental build processes.
- **Timing and power analysis:** Robust tools for timing and power analysis for more advanced technology nodes.
- **Efficient SoC integration frameworks**: Provided streamlined frameworks for system-on-chip (SoC) integration, incorporating comprehensive verification support and design-for-test capabilities.
- **Open synthetic benchmark set:** Developed a publicly available synthetic benchmark set specifically designed for the evaluation and calibration of open EDA tools, facilitating improved performance analysis and comparison.
- **Open solutions for die-to-die communication**: Delivered open technological solutions for direct die-to-die communication, conforming to industry standards and incorporating the development of associated application development kits (ADKs).
- **Advanced tools for system-in-package design**: Developed cutting-edge tools to support system-in-package (SiP) designs.
- **Standardised interfaces for design tool interoperability**: Collaborated across streams to standardise interfaces between analogue, mixed-signal, and digital design tools, improving interoperability and simplifying design workflows.
- **Prototyped tapeouts for open-source tool validation**: Demonstrated tapeouts for mainstream and advanced nodes designed with open-source tools, enabling calibration and guiding mid- to long-term priorities.
- **Enhanced formal equivalence checking**: Improved the coverage and reliability of formal equivalence checking for critical elements of the design flow.

(ii) Analogue and mixed-signal design

The overall ambition of this stream is the development of a full analogue/mixed-signal design flow. The emphasis should extend beyond improving existing tools to include the adoption of innovative approaches and new paradigms.

The following outcomes should be considered:

- **High-performance analogue and mixed-signal simulators**: Delivered advanced analogue and mixed-signal simulation tools with efficient RF simulation capabilities, incorporating techniques such as shooting Newton analysis, harmonic balance analysis, transient noise simulation, and large-signal noise simulation.
- **Advanced electromagnetic simulation tools**: Developed state-of-the-art tools for electromagnetic (EM) simulations to support complex design needs.
- **Enhanced layout tools for parasitic extraction**: Achieved fast and accurate parasitic netlist extraction from large circuit layouts, incorporating netlist reduction techniques to improve efficiency.
- **Efficient custom layout generation tools**: Provided tools for efficient custom layout generation, combining programmatic approaches with AI-assisted manual layout capabilities.
- **Standardised interfaces for tool interoperability**: Collaborated across streams to standardise interfaces between analogue, mixed-signal, and digital design tools, ensuring improved interoperability and seamless workflow integration.
- **Robust EM simulation capabilities**: Delivered comprehensive EM simulation solutions with efficient data exchange between design entry tools and circuit simulators.
- **Curated tool collections and Integrated Design Environments**: Maintained and supported curated tool collections and integrated design environments, reducing barriers to entry and enabling standardised frameworks for IP generation.
- **Open-source IP generation frameworks**: Facilitated the creation of IP under open-source licence terms, including detailed documentation, verification test benches, and silicon validation results.

(iii) Productivity, interoperability, and verification

The overarching aim of this stream is to enhance productivity by adopting innovative design approaches and ensuring seamless data exchange between tools. This will be complemented by the development of robust verification processes that accommodate diverse methodologies and effectively tackle the increasing complexity of modern chip design.

The following outcomes should be considered:

- **High-speed mixed-mode simulation tools**: Delivered advanced simulation capabilities supporting both HDL or gate-level designs and analogue components for efficient mixed-mode analysis.
- **Tailored verification environments**: Enhanced verification tools and methodologies, creating robust environments specifically designed for analogue and mixed-signal designs.
- **Improved waveform viewing tools**: Developed enhanced waveform viewing tools with features such as automated waveform analysis, backtracing functionalities, and improved usability.

- **Standardised tool interfaces for interoperability**: Collaborated across streams to standardise interfaces between analogue, mixed-signal, and digital design tools, improving interoperability and streamlining design workflows.
- **Curated tool collections for IP generation**: Maintained and supported curated tool collections and integrated design environments, reducing barriers to entry and enabling standardised processes for IP creation and management.
- **Modular frameworks for design and verification**: Developed modular frameworks enabling custom integration of design and verification transformations.
- **Open data exchange guidelines**: Established requirements and guidelines for open data exchange formats to facilitate seamless communication between tools and systems.
- **Usability improvements for open-source EDA tools**: Implemented general usability and accessibility improvements to existing open-source EDA tools, meeting the needs of a diverse user base.
- **Support for industry-standard verification**: Provided robust support for industry-standard verification methodologies, integrating them with innovative verification technologies.
- **Cross-domain verification capabilities**: Enabled effective cross-domain verification across various abstraction levels, including hardware/software co-design.

Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.
Regarding page limits:

Chapter	PO Phase	FPP Phase
Excellence	60 pages	60 pages
Impact	60 pages	100 pages
Quality and efficiency of the Implementation	60 pages	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions:

Size limit	30 Participants
Max EU Contribution per partner (% of the total EU funding)	40%

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes).

Participation is limited to legal entities established in EU Member States, Norway, Iceland, Associated Countries, OECD and Mercosur countries (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed below, but which are directly or indirectly controlled from a non-eligible country or from a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees approved by their eligible country of establishment, in so far this is a Member State or Associated Country, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Score

The scores will be given with a resolution of one decimal. The score table is for PO and FPP.

Criteria	Range	Weight (**)	Threshold (*)
Excellence	0-5	1.0	3
Impact	0-5	1.5	3
Quality and efficiency of the Implementation	0-5	0.7	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	Maximum EU Contribution as % of the Eligible Cost according to HE (*)
For profit organization but not an SME	20 %
SME (for profit SME)	30 %
University/Other (not for profit)	50 %

(*) beneficiaries may ask for a lower contribution.

3.1.5 A Pan-European infrastructure for Chips Design Innovation

Topic: HORIZON-JU-Chips-2025-CSA

Type of Action	Coordination and Support Actions (CSA)
Indicative EU budget	12 M€
Expected EU contribution per project	12 M€
Mode	EU funding only One stage Call, with submission of Full Project Proposal (FPP)
Call launch date	04 March 2025
Deadline FPP	29 Apr 2025 at 17:00 Brussels Time

Context

This call relates to the second general objective of the Chips JU: "build up large-scale design capacities for integrated semiconductor technologies"; and the seventh objective: "foster a dynamic Union-wide ecosystem based on digital value chains with simplified access to newcomers", including the active involvement of Academia, RTOs, and SMEs. This call aims at supporting the follow-up, extension and consolidation of EUROPRACTICE services to provide Europe with an open-access platform to design and fabricate chips.

Expected Outcomes

Proposals are expected to address the following expected outcomes:

Here are the outcomes with the title capitalisation removed in the bold parts:

- **Establish a platform for the European design ecosystem**: Created a platform that supports the growth of a European design ecosystem by fostering design reuse, enabling the exploitation of advanced technologies in various application domains, and providing a foundation for deep-tech startups.
- **Encourage dissemination of PDKs through the platform**: Actively supported foundries in sharing open-source and proprietary technologies, particularly their PDKs, via the platform.
- **Streamline access to EDA tools**: Simplified and lowered barriers to access commercial and open-source industry-standard EDA tools across various technologies, with a focus on affordability.

- **Enhance workforce skills through hands-on experience**: Reduced barriers for undergraduate and postgraduate students to gain hands-on IC design experience, complementing their theoretical coursework.
- **Provide diverse chip design flows**: Offered a variety of chip design flows, supporting multi-vendor configurations where feasible, and assisted users in customising their design workflows.
- **Facilitate affordable prototyping access**: Enabled academia, research centres, and spinouts to prototype affordably using industrial-grade and emerging technologies, including advanced nodes, mature nodes, open-source solutions, and pilot-line technologies, with pathways to volume production.
- **Offer extensive training resources**: Delivered comprehensive training resources to up-skill and re-skill students and professionals across a wide range of technologies.
- **Train academics and instructors through 'train-the-trainer' programmes**: Provided targeted training for educators in semiconductor and photonics technologies to improve teaching quality and dissemination.
- **Provide a platform for open-source IP exchange**: Established a platform for sharing open-source IP, fostering collaboration and reuse.
- **Support students in gaining hands-on chip design experience**: Facilitated pre-tertiary and vocational students' access to open-source tool flows, promoting practical engagement with chip design.
- **Ensure access to customer support and leading-edge tools**: Simplified access to customer support, IP, and cutting-edge design tools for a broad user base.
- **Lower barriers for advanced packaging and integration**: Supported users in adopting advanced packaging and heterogeneous integration techniques by reducing entry barriers.
- **Enable efficient fabrication and system integration**: Facilitated multi-project wafer (MPW) runs and small-volume fabrication of ASICs, photonics, MEMS, sensors, and their integration at the system level, while promoting the adoption of emerging or underutilised technologies such as quantum technologies, photonics, and wide-bandgap materials by academia and SMEs.
- **Promote technology offerings from research centres**: Supported and highlighted the technology services of research centres with lower TRL (technology readiness level) capabilities.

    - Furthermore, particular emphasis should be placed on ensuring the seamless integration of this initiative within the framework of the Chips Act. To this end, proposals must address the following outcomes:

- Collaborate extensively with initiatives under Pillar 1 of the Chips Act such as the Design Platform, competence centres and pilot lines. Particularly by:
    i. collaborating extensively with the Design Platform initiative, including through joint activities;
    ii. facilitating academic access to the Chips Act pilot lines;
    iii. support competence centres across all EU Member States.
- Implement a comprehensive plan to **integrate EUROPRACTICE services into the Chips Act's Design Platform before the conclusion of this project**.

Scope

Semiconductors are at the centre of strong geostrategic interests, and at the core of the global technological race. A priority for Europe is to strengthen its design capacity and to lower the barriers to get access to advanced semiconductor technologies. Amongst others, this requires the nurturing and supply of people with the right digital skills, and the provision of routes to prototype and commercialisation. Not only large enterprises, but also startups and academic institutions play a key role and are crucial in the European semiconductor value chain.

Proposals need to lower the entry-barrier for academia, research institutes and very importantly for startups, and SMEs by offering affordable access to a portfolio of industrial-grade design tools, IP blocks, including open-source ones (e.g. RISC-V based), and prototyping technologies. Services offered must include initial advice, training, support, reduced entry costs, prototyping and a clear route to chip manufacture and product supply. Proposals should include a KPI on start-ups and SMEs that use the services provided by the platform.

Furthermore, proposals should include some of the following elements:

- Fostering collaboration and support in Europe by providing a design IP exchange system, where members can exchange IP blocks, including commercialisation of academic designs, considering national rules if relevant.
- Supporting and stimulating the adoption of emerging technologies (e.g. neuromorphic, 3D integration, wafer-scale-packaging etc) by creating standardised platforms and make those widely accessible;
- Enabling heterogeneous system integration, such as the adoption of chiplets by a wide range of customers.
- Strengthening industry relevant skills by supporting up-skilling and re-skilling initiatives through provision of extended training activities.
- Integrating the initiative into the broader framework of the Chips Act.

Reminding that of general importance to the Chips JU calls are:

- Re-use of results from previous ECSEL/Chips JU, H2020 or EUREKA-cluster projects is encouraged.
- Developing synergies with other relevant European, national or regional initiatives and/or funding programmes.
- Encouraging SMEs to participate in those developments, in particular paying attention to the needs of SMEs, involve SMEs in project execution, and develop solutions that can be taken up and/or exploited by SMEs.

In this topic the integration of the gender dimension (sex and gender analysis) in research and innovation content is not a mandatory requirement.

Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Regarding page limits:

- The page limit for the chapter EXCELLENCE is 30 pages.
- The page limit for the chapter QUALITY AND EFFICIENCY OF THE IMPLEMENTATION is 30 pages.
- The page limit for the chapter IMPACT is 30 pages.

Eligibility

Applications will only be considered eligible if their content corresponds wholly (or at least in part) to the topic description for which they are submitted.

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes).

Financial and operational capacity and exclusion

Please refer to Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Score

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Excellence	0-5	1	3
Impact	0-5	1	3
Quality and efficiency of the Implementation	0-5	1	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to Horizon Europe.

Type of beneficiary	EU Contribution as % of the Eligible Cost according to HE
For profit organization but not an SME	100 %
SME (for profit SME)	100 %
University/Other (not for profit)	100 %

3.1.6 Low power Edge AI Chips

Topic: DIGITAL-Chips-2025-1-IA-LEAI

Type of Action	Simple Grant
Indicative EU budget	20 M€
Expected EU contribution per project	The JU estimates that an EU contribution of between EUR 4 and 5 million would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Co-funded with the NFA One stage Call with submission of Full Proposal (FPP)
Call launch date	08 July 2025
Deadline FPP Phase	17 Sep 2025 at 17:00 Brussels Time

Expected Outcomes

Successful proposals are expected to deliver the following outcomes:

- Develop AI chip prototypes reaching TRL 6-7, integrating cutting-edge technologies such as non-volatile memories, neuromorphic computing, 3D heterogeneous integration, and photonic connectivity. These prototypes should be tested under real-world conditions and show potential for industrial scaling.
- Leverage the advanced capabilities of state-of-the-art infrastructures with fabrication and testing capabilities available within the Union, especially at leading Research and Technology Organisations (RTOs). This includes utilizing the Testing and Experimentation Facility (TEF) for Edge AI hardware (PREVAIL project[23]), a platform designed to accelerate the development of cutting-edge AI solutions, as well as Pilot Lines, including the ones of the Chips for Europe Initiative.
- The prototypes should demonstrate robust AI capabilities, including real-time inference, on-device learning, and adaptive decision-making. This enables edge AI

[23] https://prevail-project.eu/

systems to process data locally, make decisions, and adapt to changing environments without relying on cloud infrastructure, reducing latency and power consumption.

- The prototypes must achieve ultra-low power consumption to ensure energy-efficient AI operations in power-constrained edge environments, particularly for battery-powered devices. The emphasis should be on balancing computing power with energy efficiency.
- By advancing AI chips that are energy-efficient and highly secure, the developed technologies should contribute to Europe's digital transformation and help meet sustainability goals.

The ultimate goal of the project should be to drive the development of next-generation edge AI chips that combine high performance with ultra-low power consumption. These chips will enable real-time, on-chip AI capabilities for applications in fields like mobile communication networks (e.g. 6G), autonomous systems, industrial automation, and healthcare, all while aligning with Europe’s sustainability and digitalization goals.

Scope

Proposals to this call should target the development of next-generation edge AI chips, specifically delivering high-performance, ultra-low-power AI hardware solutions for applications at the edge of the network. The main scope should be to develop, test, and prototype next-generation edge AI technologies leveraging the advanced capabilities of state-of-the-art infrastructure available in the Union, such as the Testing and Experimentation Facility (TEF) for Edge AI hardware (PREVAIL project) as well as Pilot Lines, including the ones of the Chips for Europe Initiative. The objective is to accelerate the transition of advanced ultra-low power edge computing technologies “from the lab to the fab”, harnessing the facilities of leading European research and technology organizations.

The proposed edge AI chips should be based on technologies that overcome the memory bottlenecks of classical “Von Neumann” computing architecture, enabling substantial performance gains, including:

- Solutions for computing in-memory, using Non-Volatile Embedded Memories, such as Magnetoresistive Random Access Memory (MRAM), Oxide-based RAM (OxRAM), and Ferroelectric RAM (FeRAM) technologies. critical for achieving energy-efficient AI processing by enabling fast, low-power data storage and retrieval.
- Unconventional architectures for neuromorphic and analogue computing, mimicking the brain's neural networks by employing alternative AI approaches such as spiking neural networks (SNNs) artificial neural networks based on magnetic tunnel junctions (MTJ)and specialized materials, thereby enabling real-time on-chip sensing, learning and inference with extremely low energy overhead, drastically reducing power consumption.

- Advanced 3D integration and packaging technologies for the efficient integration of heterogeneous components (such as memory, computing, and I/O) into a single compact chip. By using interposer technologies, die-to-wafer, wafer-to-wafer, and Through-Silicon Via (TSV) techniques, chip prototypes can reduce the overall system footprint, improving performance and energy efficiency.
- Photonic Integrated Circuits (PICs) for ultrafast, energy-efficient artificial neural networks, enhancing both computational efficiency and data transfer speeds with low latency, ideal to ensure reliable high-speed connectivity in telecommunication networks and connected devices.

Proposals should target TRL 6-7 and demonstrate advancements in AI processing for real-time applications, while maintaining an emphasis on energy efficiency.

Consortia should be focussed on the realisation of the final prototype(s) and each partner should have a well-defined essential role towards the achievement of the objectives. Therefore, consortia are suggested to include strictly the participants that are required to cover the necessary tasks.

Admissibility

Admissibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Regarding page limits:

Chapter	PO Phase	FPP Phase
Relevance	60 pages	60 pages
Implementation	60 pages	100 pages
Impact	60 pages	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

Eligibility

Eligibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Specific eligibility conditions:

Size limit	70 Participants
Max EU Contribution per partner (% of the total EU funding)	50 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to participation restrictions for the protection of European digital infrastructures, communication and information systems, and related supply chains, as described in Annex 4 of the WP General Annexes.

Legal entities that are established in the Union or EEA countries but are controlled from third countries may only participate on the condition that they guarantee the protection of the essential security interests of the Union and the Member States and that they ensure the protection of classified documents information. Where applicable, security guarantees need to be provided after proposal selection.

Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Award criteria.

Please refer to Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes

Specific rules may apply regarding the eligibility to national funding.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Scores

The scores will be given with a resolution of one decimal.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Relevance	0-5	1.0	3

Implementation	0-5	1.0	3
Impact	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to DEP.

Type of beneficiary	**Maximum EU Contribution as % of the Eligible Cost according to DEP (*)**
For profit organization but not an SME	25 %
SME (for profit SME)	35 %
University/Other (not for profit)	35 %

(*) beneficiaries may ask for a lower contribution.

3.2 Accelerator for Advanced Strained Silicon on Insulator Substrates

Topic: DIGITAL-JU-Chips-2025-SG-SSOI

Type of Action	Simple Grant
Indicative EU budget	30 M€
Expected EU contribution per project	30 M€
Mode	Co-funded with the NFA One stage, with submission of Full Project Proposal (FPP)
Call launch date	08 Jul 2025
Deadline FPP	20 November 2025 at 17:00 Brussels Time

Context

The continuous demand for higher-performing, energy-efficient semiconductor devices is driving the need for innovation in substrate engineering. Industries such as telecommunications, automotive, and consumer electronics require advanced solutions that can meet the growing complexity of applications like 5G/6G communications, autonomous driving, and edge AI/ML computing. As conventional silicon technologies approach their physical limits in terms of speed, power efficiency, and miniaturisation, Strained Silicon on Insulator (sSOI) substrates are emerging as a key enabler of the next generation of semiconductor devices. By introducing strain into the silicon layer, sSOI enhances electron mobility, offering significant performance gains in advanced nodes such as 7nm FD-SOI.

FD-SOI technology is already a vital asset for Europe, offering an excellent balance between power consumption, speed, and cost. However, as the technology scales down to the 7nm node, integrating sSOI substrates becomes essential to maintain these advantages. The unique properties of sSOI effectively address the challenges posed by smaller transistor sizes, enabling improved energy efficiency and sustained high performance. This makes sSOI a crucial component in meeting the demands of Europe's key markets, including mobile and infrastructure, automotive sensors, and IoT devices.

To bridge the gap between research breakthroughs and industrial-scale production, there is an urgent need for a dedicated accelerator that can handle the complexities of sSOI substrate

development. Current R&D pilot lines lack the capacity and scale required to produce the thousands of wafers needed to ensure low defect densities and high manufacturing yields. An accelerator is essential to enable this transition, ensuring that sSOI substrates can meet the rigorous requirements for integration into advanced FD-SOI manufacturing processes.

This accelerator will provide the necessary infrastructure to validate sSOI substrates on an industrial scale, accelerating their adoption within the European semiconductor ecosystem. By supporting high-volume production, manufacturers can assess the feasibility and cost-effectiveness of sSOI in large-scale FD-SOI applications. This initiative will reinforce Europe's leadership in semiconductor innovation, ensuring the industry remains competitive in the global market for advanced devices.

Moreover, the accelerator will foster collaboration across the semiconductor value chain—from material providers to foundries and system integrators. This cooperation will reduce the risks associated with new substrate technologies and promote the rapid commercialization of sSOI-based solutions. In doing so, it will contribute to Europe's strategic goals of technological sovereignty and sustainability in key high-performance sectors.

Scope

The proposed accelerator should address all levels of the key technological steps required to bring sSOI substrates to industrial scale:

- **Development of industrial-grade sSOI substrates** will focus on achieving low defect density, crucial for enhancing electron mobility and ensuring high-performance FD-SOI devices at the 7 nm node. This will involve refining **strain engineering techniques**, particularly to introduce a uniform global strain that can balance the performance for strained NMOS and relaxed PMOS transistors.
- Ensure compatibility with existing semiconductor manufacturing, the accelerator will refine **process integration and optimisation**. This includes improving epitaxial growth, wafer bonding, and defect reduction techniques to meet the requirements of advanced FD-SOI production processes.

  Finally, the accelerator will **promote collaboration** across the semiconductor ecosystem, working with other pilot lines, as well as connecting to the design platform and competence centres, among others.

Expected Outcomes

The proposed accelerator should be established with all the necessary equipment and facilities, and will target the following main **objectives**:

- Develop **industrial-grade sSOI substrates** with reduced defect density to improve **electron mobility** and overall device performance. These substrates should be capable of addressing the market entry of 7nm FD-SOI expected by 2030 as well as be fully compatible with existing FD-SOI technologies, including 22FDX and 18nm FD-SOI.
- **Develop scalable and cost-effective manufacturing processes,** ensuring compatibility with current industrial standards and promoting widespread adoption.
- Demonstrate the feasibility of integrating **strained NMOS and relaxed PMOS areas**, balancing the performance of both transistors.
- Accelerate the transition from R&D to industrial-scale production by providing a pre-industrial infrastructure capable of **producing several thousand wafers per year**.
- **Develop demonstrators** to validate the benefits of sSOI-based FD-SOI over competing FinFET technologies, particularly in terms of improved RF performance, lower noise, and reduced power consumption.
- Enable open access to Process Design Kits (PDKs) and design building blocks to foster the differentiation of FD-SOI technology, including stress and relaxation design elements.
- Enable early-stage design and system-level integration of sSOI substrates through Multi-Project Wafer (MPW) runs, allowing timely validation of substrate performance in real-world applications. Support design efforts for high-speed broadband RF circuits, mm-Wave radar systems, and compact low power automotive and IoT solutions as part of the Next Gen FD-SOI roadmap.

The **expected results** for this accelerator should therefore comprise:

- Create a **sustainable accelerator open to all European stakeholders**, providing access to state-of-the-art sSOI technology and manufacturing capabilities.
- **Develop and standardize Process Design Kits** based on validated sSOI substrate data, enabling designers to optimise their system-level architectures and meet the demands of next-generation applications. These PDKs should support the transition to 7nm FD-SOI technology, ensuring readiness for high-volume manufacturing by 2030.
- Expand the capabilities of sSOI substrates to **industrial-scale wafer production**, ensuring low defect densities and improved manufacturing yields that meet the rigorous standards of advanced semiconductor fabrication.
- Drive the creation of **intellectual property** and strengthen Europe's production capacity in sSOI technologies, contributing to Europe's leadership in critical semiconductor markets.
- With a particular focus on complementarity with the FD-SOI pilot line, foster collaborative development through **synergies with other Chips JU pilot lines**, enhancing the overall innovation capacity and technological leadership of Europe in semiconductor technologies,

- Provide comprehensive **training programs and skill development** initiatives to equip European technologists and engineers with the expertise necessary for sSOI substrate integration and advanced semiconductor manufacturing.

Admissibility

Admissibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Regarding page limits:

Chapter	FPP Phase
Relevance	60 pages
Implementation	100 pages
Impact	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

Eligibility

Eligibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Specific eligibility conditions:

Size limit	70 Participants
Max EU Contribution per partner (% of the total EU funding)	50 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to participation restrictions for the protection of European digital infrastructures, communication and information systems, and related supply chains, as described in Annex 4 of the WP General Annexes.

Legal entities that are established in the Union or EEA countries but are controlled from third countries may only participate on the condition that they guarantee the protection of the

essential security interests of the Union and the Member States and that they ensure the protection of classified documents information. Where applicable, security guarantees need to be provided after proposal selection.

Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Evaluation procedure

For the specificity of each call evaluation please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Award criteria.

Please refer to Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes

Specific rules may apply regarding the eligibility to national funding.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Score

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Relevance	0-5	1.0	3
Implementation	0-5	1.0	3
Impact	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to DIGITAL.

Type of beneficiary	EU Contribution as % of the Eligible Cost according to DIGITAL (*)
For profit organization but not an SME	25 %
SME (for profit SME)	35 %
University/Other (not for profit)	35 %

(*) beneficiaries may ask for a lower contribution.

3.3 Quantum Chips

3.3.1 Supporting developing Quantum Chip Technology for superconducting stability Pilot

Topic: HORIZON-JU-Chips-2025-QAC1-1-SGA

Type of Action	RIA Specific grant agreement in relation to a Framework Partnership Agreement
Indicative EU budget	25 M€
Expected EU contribution per project	25 M€
Mode	Co-funded with the NFA One stage, with submission of Full Project Proposal (FPP)
Invitation date	30th July 2025
Deadline FPP	17th September 2025

Context

Within the Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots, the selected consortia will be invited to submit a proposal that will implement the first 3-4 years of the action plan for providing stable pilot fabrication capabilities defined in the FPA that would foster quantum chips production and rapid innovation tailored to meet the needs of the European quantum industry over the next decade, in particular start-ups and SMEs. The testing and experimentation facilities should be fully integrated in the pilots, providing seamless production and testing services.

Expected outcomes.

The proposal should aim to establish superconducting stability pilot production capabilities for a first of their kind quantum technology, where in the future European companies, research centres and academic institutions can produce quantum chips on a stable pilot scale based on a shared cost model between users and service providers. The targeted stability pilot should have a simple baseline process ready in 2-3 years from start of the project - reaching at least Technology Readiness Level (TRL) 6.

An early industrialization roadmap should be available by month 6 of the project, with the expectation that it will be regularly updated throughout the project's lifetime to incorporate evolving technical progress, market needs, and alignment with industrial partner requirements for scaling and commercialization towards mass production.

The proposal should focus on developing scalable production processes for quantum chips, with the goal of establishing industrial-level manufacturing methods. This includes the integration of cutting-edge Quantum Process Design Kits (PDKs) with the European Design Platform, aiming to standardize production workflows and minimize the need for custom developments. The proposal should include enabling technologies for quantum chips, namely advanced tools, components, and systems that facilitate the design, fabrication, operation, testing, and scaling of these devices. However, it should not include activities aimed at developing other essential components or subsystems that are unrelated or not directly integrated with the quantum chips. The initiative should seek to enhance technology and manufacturing readiness levels across the quantum industry, targeting applications in quantum computing, communications, simulations, and sensing. A key objective should be to establish standardized methodologies for the design, testing, and manufacturing of quantum chips, ensuring efficient production processes and broadening the range of applications in various sectors.

Key milestones should be clearly defined, with ambitious and technology-specific KPIs such as high yield, high-quality quantum chips, reliability, reproducibility, performance, and scalability of production. In addition, the proposal is expected to appropriately address the shortcomings identified in the Evaluation Summary Report of the corresponding FPA awarded under topic Chips-QAC-1, as appropriate to the relevant activities in the current SGA phase.

The proposal should demonstrate scalable, efficient, and stable production capabilities, with a focus on achieving high yield and consistency in quantum chip manufacturing. This will involve developing robust, repeatable manufacturing processes tailored to the unique requirements of superconducting quantum chips, ensuring a reliable supply chain for European stakeholders. Additionally, the proposal should outline the development of reliable characterization tools to ensure quality assurance, demonstrating the scalability of pilot technologies from small-to-mid volume fabrication to large-scale industrial production. A comprehensive technology roadmap and implementation plan should be defined to guide the industrialization of quantum chip production in the future and ensure the sustainability and growth of the quantum industry.

Scope

The action will require expertise in the area of manufacturing flows for quantum technologies, in particular in quantum computing/simulation (e.g. qubit fabrication), communication and sensing, and with issues regarding high-quality, reliability, versatility, process control including integrated testing and minimizing lead times. Interaction with standardisation bodies and data sharing on benchmarking is also encouraged.

The proposal should also cover: (i) the collaboration with other initiatives or programmes at regional, national, or European level such as Framework Partnership Agreements (FPAs) awarded under topic Chips-QAC-2: Call for establishing Framework Partnership Agreement(s) for developing Quantum Chip Technology for high-quality Stability Pilots, and the relevant Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots. This includes synergies and cooperation with the experimental pilot lines QU-PILOT and QU-TEST of the Quantum Flagship Initiative, for R&D support; (ii) any additional financial support they may receive in their activities from relevant national or regional initiatives.

In this topic the integration of the gender dimension (sex and gender analysis) in research and innovation content is not a mandatory requirement.

Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Regarding page limits:

Chapter	**FPP Phase**
Excellence	60 pages
Impact	100 pages
Quality and efficiency of the Implementation	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions:

Max Contribution per partner (% of the total EU funding): 40 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes for details).

Participation is limited to legal entities established in EU Member States, Norway, Iceland, and Israel (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled from a non-eligible country or from a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees approved by their eligible country of establishment, in so far this is a Member State or Associated Country, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Score

The scores will be given with a resolution of one decimal.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Excellence	0-5	1.0	3
Impact	0-5	1.0	3
Quality and efficiency of the Implementation	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	**Maximum EU Contribution as % of the Eligible Cost according to HE (*)**
For profit organization but not an SME	50 %
SME (for profit SME)	50 %
University/Other (not for profit)	50 %

(*) beneficiaries may ask for a lower contribution.

Purchases of equipment or other assets used for the action must be declared as depreciation costs. However, costs may exceptionally be declared as full capitalised costs for high-value equipment that is essential for the development of the pilots, particularly where such equipment contributes to the development of an EU ecosystem of equipment providers and users, and ultimately to European technological autonomy. This exception may apply where the equipment represents a significant share of the beneficiary's eligible costs and where limiting the cost to depreciation would introduce delays in the implementation or compromise project objectives. The list of eligible items to be declared as full capitalised costs, should be part of the proposal and will be confirmed by the Chips JU during the grant preparation process.

STEP and Sovereignty Seal

This topic contributes to the objectives of the *Strategic Technologies for Europe Platform* (STEP). As such, eligible proposals that exceed the evaluation thresholds will be awarded a *Sovereignty Seal*. The Sovereignty Seal is a quality label, valid for the duration of the project, which will facilitate access to additional EU funding (alternative, cumulative or combined funding from several EU budget instruments) or national public and private investments.

3.3.2 Supporting developing Quantum Chip Technology for photonic stability Pilot

Topic: HORIZON-JU-Chips-2025-QAC1-2-SGA

Type of Action	RIA Specific grant agreement in relation to a Framework Partnership Agreement
Indicative EU budget	25 M€
Expected EU contribution per project	25 M€
Mode	Co-funded with the NFA One stage, with submission of Full Project Proposal (FPP)
Invitation date	30th July 2025
Deadline FPP	17th September 2025

Context

Within the Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots, the selected consortia will be invited to submit a proposal that will implement the first 3-4 years of the action plan for providing stable pilot fabrication capabilities defined in the FPA that would foster quantum chips production and rapid innovation tailored to meet the needs of the European quantum industry over the next decade, in particular start-ups and SMEs. The testing and experimentation facilities should be fully integrated in the pilots, providing seamless production and testing services.

Expected outcomes.

The proposal should aim to establish photonic stability pilot production capabilities for a first of their kind quantum technology, where in the future European companies, research centres and academic institutions can produce quantum chips on a stable pilot scale based on a shared cost model between users and service providers. The targeted stability pilot should have a simple baseline process ready in 2-3 years from start of the project - reaching at least Technology Readiness Level (TRL) 6.

An early industrialization roadmap should be available by month 6 of the project, with the expectation that it will be regularly updated throughout the project's lifetime to incorporate

evolving technical progress, market needs, and alignment with industrial partner requirements for scaling and commercialization towards mass production.

The proposal should focus on developing scalable production processes for quantum chips, with the goal of establishing industrial-level manufacturing methods. This includes the integration of cutting-edge Quantum Process Design Kits (PDKs) with the European Design Platform, aiming to standardize production workflows and minimize the need for custom developments. The proposal should include enabling technologies for quantum chips, namely advanced tools, components, and systems that facilitate the design, fabrication, operation, testing, and scaling of these devices. However, it should not include activities aimed at developing other essential components or subsystems that are unrelated or not directly integrated with the quantum chips. The initiative should seek to enhance technology and manufacturing readiness levels across the quantum industry, targeting applications in quantum computing, communications, simulations, and sensing. A key objective should be to establish standardized methodologies for the design, testing, and manufacturing of quantum chips, ensuring efficient production processes and broadening the range of applications in various sectors.

Key milestones should be clearly defined, with ambitious and technology-specific KPIs such as high yield, high-quality quantum chips, reliability, reproducibility, performance, and scalability of production. In addition, the proposal is expected to appropriately address the shortcomings identified in the Evaluation Summary Report of the corresponding FPA awarded under topic Chips-QAC-1, as appropriate to the relevant activities in the current SGA phase.

The proposal should demonstrate scalable, efficient, and stable production capabilities, with a focus on achieving high yield and consistency in quantum chip manufacturing. This will involve developing robust, repeatable manufacturing processes tailored to the unique requirements of photonic quantum chips, ensuring a reliable supply chain for European stakeholders. Additionally, the proposal should outline the development of reliable characterization tools to ensure quality assurance, demonstrating the scalability of pilot technologies from small-to-mid volume fabrication to large-scale industrial production. A comprehensive technology roadmap and implementation plan should be defined to guide the industrialization of quantum chip production in the future and ensure the sustainability and growth of the quantum industry.

Scope

The action will require expertise in the area of manufacturing flows for quantum technologies, in particular in quantum computing/simulation (e.g. qubit fabrication), communication and sensing, and with issues regarding high-quality, reliability, versatility, process control including integrated testing and minimizing lead times. Interaction with standardisation bodies and data sharing on benchmarking is also encouraged.

The proposal should also cover: (i) the collaboration with other initiatives or programmes at regional, national, or European level such as Framework Partnership Agreements (FPAs) awarded under topic Chips-QAC-2: Call for establishing Framework Partnership Agreement(s)

for developing Quantum Chip Technology for high-quality Stability Pilots, and the relevant Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots. This includes synergies and cooperation with the experimental pilot lines QU-PILOT and QU-TEST of the Quantum Flagship Initiative, for R&D support; (ii) any additional financial support they may receive in their activities from relevant national or regional initiatives.

In this topic the integration of the gender dimension (sex and gender analysis) in research and innovation content is not a mandatory requirement.

Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Regarding page limits:

Chapter	**FPP Phase**
Excellence	60 pages
Impact	100 pages
Quality and efficiency of the Implementation	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions:

Max Contribution per partner (% of the total EU funding): 40 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes for details).

Participation is limited to legal entities established in EU Member States, Norway, Iceland, and Israel (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled from a non-eligible country or from a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees approved by their eligible country of establishment, in so far this is a Member State or Associated Country, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Score

The scores will be given with a resolution of one decimal.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Excellence	0-5	1.0	3
Impact	0-5	1.0	3
Quality and efficiency of the Implementation	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	Maximum EU Contribution as % of the Eligible Cost according to HE (*)
For profit organization but not an SME	50 %
SME (for profit SME)	50 %
University/Other (not for profit)	50 %

(*) beneficiaries may ask for a lower contribution.

Purchases of equipment or other assets used for the action must be declared as depreciation costs. However, costs may exceptionally be declared as full capitalised costs for high-value equipment that is essential for the development of the pilots, particularly where such equipment contributes to the development of an EU ecosystem of equipment providers and users, and ultimately to European technological autonomy. This exception may apply where the equipment represents a significant share of the beneficiary's eligible costs and where limiting the cost to depreciation would introduce delays in the implementation or compromise project objectives. The list of eligible items to be declared as full capitalised costs must be part of the proposal and will be confirmed by the Chips JU during the grant preparation process.

STEP and Sovereignty Seal

This topic contributes to the objectives of the *Strategic Technologies for Europe Platform* (STEP). As such, eligible proposals that exceed the evaluation thresholds will be awarded a *Sovereignty Seal*. The Sovereignty Seal is a quality label, valid for the duration of the project, which will facilitate access to additional EU funding (alternative, cumulative or combined funding from several EU budget instruments) or national public and private investments.

3.3.3 Supporting developing Quantum Chip Technology for semiconducting stability Pilot

Topic: HORIZON-JU-Chips-2025-QAC1-3-SGA

Type of Action	RIA Specific grant agreement in relation to a Framework Partnership Agreement
Indicative EU budget	25 M€
Expected EU contribution per project	25 M€
Mode	Co-funded with the NFA One stage, with submission of Full Project Proposal (FPP)
Invitation date	30th July 2025
Deadline FPP	17th September 2025

Context

Within the Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots, the selected consortia will be invited to submit a proposal that will implement the first 3-4 years of the action plan for providing stable pilot fabrication capabilities defined in the FPA that would foster quantum chips production and rapid innovation tailored to meet the needs of the European quantum industry over the next decade, in particular start-ups and SMEs. The testing and experimentation facilities should be fully integrated in the pilots, providing seamless production and testing services.

Expected outcomes.

The proposal should aim to establish semiconducting stability pilot production capabilities for a first of their kind quantum technology, where in the future European companies, research centres and academic institutions can produce quantum chips on a stable pilot scale based on a shared cost model between users and service providers. The targeted stability pilot should have a simple baseline process ready in 2-3 years from start of the project - reaching at least Technology Readiness Level (TRL) 6.

An early industrialization roadmap should be available by month 6 of the project, with the expectation that it will be regularly updated throughout the project's lifetime to incorporate

evolving technical progress, market needs, and alignment with industrial partner requirements for scaling and commercialization towards mass production.

The proposal should focus on developing scalable production processes for quantum chips, with the goal of establishing industrial-level manufacturing methods. This includes the integration of cutting-edge Quantum Process Design Kits (PDKs) with the European Design Platform, aiming to standardize production workflows and minimize the need for custom developments. The proposal should include enabling technologies for quantum chips, namely advanced tools, components, and systems that facilitate the design, fabrication, operation, testing, and scaling of these devices. However, it should not include activities aimed at developing other essential components or subsystems that are unrelated or not directly integrated with the quantum chips. The initiative should seek to enhance technology and manufacturing readiness levels across the quantum industry, targeting applications in quantum computing, communications, simulations, and sensing. A key objective should be to establish standardized methodologies for the design, testing, and manufacturing of quantum chips, ensuring efficient production processes and broadening the range of applications in various sectors.

Key milestones should be clearly defined, with ambitious and technology-specific KPIs such as high yield, high-quality quantum chips, reliability, reproducibility, performance, and scalability of production. In addition, the proposal is expected to appropriately address the shortcomings identified in the Evaluation Summary Report of the corresponding FPA awarded under topic Chips-QAC-1, as appropriate to the relevant activities in the current SGA phase.

The proposal should demonstrate scalable, efficient, and stable production capabilities, with a focus on achieving high yield and consistency in quantum chip manufacturing. This will involve developing robust, repeatable manufacturing processes tailored to the unique requirements of semiconducting quantum chips, ensuring a reliable supply chain for European stakeholders. Additionally, the proposal should outline the development of reliable characterization tools to ensure quality assurance, demonstrating the scalability of pilot technologies from small-to-mid volume fabrication to large-scale industrial production. A comprehensive technology roadmap and implementation plan should be defined to guide the industrialization of quantum chip production in the future and ensure the sustainability and growth of the quantum industry.

Scope

The action will require expertise in the area of manufacturing flows for quantum technologies, in particular in quantum computing/simulation (e.g. qubit fabrication), communication and sensing, and with issues regarding high-quality, reliability, versatility, process control including integrated testing and minimizing lead times. Interaction with standardisation bodies and data sharing on benchmarking is also encouraged.

The proposal should also cover: (i) the collaboration with other initiatives or programmes at regional, national, or European level such as Framework Partnership Agreements (FPAs) awarded under topic Chips-QAC-2: Call for establishing Framework Partnership Agreement(s)

for developing Quantum Chip Technology for high-quality Stability Pilots, and the relevant Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots. This includes synergies and cooperation with the experimental pilot lines QU-PILOT and QU-TEST of the Quantum Flagship Initiative, for R&D support; (ii) any additional financial support they may receive in their activities from relevant national or regional initiatives.

In this topic the integration of the gender dimension (sex and gender analysis) in research and innovation content is not a mandatory requirement.

Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Regarding page limits:

Chapter	**FPP Phase**
Excellence	60 pages
Impact	100 pages
Quality and efficiency of the Implementation	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions:

Max Contribution per partner (% of the total EU funding): 40 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes for details).

Participation is limited to legal entities established in EU Member States, Norway, Iceland, and Israel (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled from a non-eligible country or from a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees approved by their eligible country of establishment, in so far this is a Member State or Associated Country, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Score

The scores will be given with a resolution of one decimal.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Excellence	0-5	1.0	3
Impact	0-5	1.0	3
Quality and efficiency of the Implementation	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	Maximum EU Contribution as % of the Eligible Cost according to HE (*)
For profit organization but not an SME	50 %
SME (for profit SME)	50 %
University/Other (not for profit)	50 %

(*) beneficiaries may ask for a lower contribution.

Purchases of equipment or other assets used for the action must be declared as depreciation costs. However, costs may exceptionally be declared as full capitalised costs for high-value equipment that is essential for the development of the pilots, particularly where such equipment contributes to the development of an EU ecosystem of equipment providers and users, and ultimately to European technological autonomy. This exception may apply where the equipment represents a significant share of the beneficiary's eligible costs and where limiting the cost to depreciation would introduce delays in the implementation or compromise project objectives. The list of eligible items to be declared as full capitalised costs must be part of the proposal and will be confirmed by the Chips JU during the grant preparation process.

STEP and Sovereignty Seal

This topic contributes to the objectives of the *Strategic Technologies for Europe Platform* (STEP). As such, eligible proposals that exceed the evaluation thresholds will be awarded a *Sovereignty Seal*. The Sovereignty Seal is a quality label, valid for the duration of the project, which will facilitate access to additional EU funding (alternative, cumulative or combined funding from several EU budget instruments) or national public and private investments.

3.3.4 Supporting developing Quantum Chip Technology for diamond-based stability Pilot

Topic: HORIZON-JU-Chips-2025-QAC1-4-SGA

Type of Action	RIA Specific grant agreement in relation to a Framework Partnership Agreement
Indicative EU budget	25 M€
Expected EU contribution per project	25 M€
Mode	Co-funded with the NFA One stage, with submission of Full Project Proposal (FPP)
Invitation date	30th July 2025
Deadline FPP	17th September 2025

Context

Within the Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots, the selected consortia will be invited to submit a proposal that will implement the first 3-4 years of the action plan for providing stable pilot fabrication capabilities defined in the FPA that would foster quantum chips production and rapid innovation tailored to meet the needs of the European quantum industry over the next decade, in particular start-ups and SMEs. The testing and experimentation facilities should be fully integrated in the pilots, providing seamless production and testing services.

Expected outcomes.

The proposal should aim to establish diamond-based stability pilot production capabilities for a first of their kind quantum technology, where in the future European companies, research centres and academic institutions can produce quantum chips on a stable pilot scale based on a shared cost model between users and service providers. The targeted stability pilot should have a simple baseline process ready in 2-3 years from start of the project - reaching at least Technology Readiness Level (TRL) 6.

An early industrialization roadmap should be available by month 6 of the project, with the expectation that it will be regularly updated throughout the project's lifetime to incorporate

evolving technical progress, market needs, and alignment with industrial partner requirements for scaling and commercialization towards mass production.

The proposal should focus on developing scalable production processes for quantum chips, with the goal of establishing industrial-level manufacturing methods. This includes the integration of cutting-edge Quantum Process Design Kits (PDKs) with the European Design Platform, aiming to standardize production workflows and minimize the need for custom developments. The proposal should include enabling technologies for quantum chips, namely advanced tools, components, and systems that facilitate the design, fabrication, operation, testing, and scaling of these devices. However, it should not include activities aimed at developing other essential components or subsystems that are unrelated or not directly integrated with the quantum chips. The initiative should seek to enhance technology and manufacturing readiness levels across the quantum industry, targeting applications in quantum computing, communications, simulations, and sensing. A key objective should be to establish standardized methodologies for the design, testing, and manufacturing of quantum chips, ensuring efficient production processes and broadening the range of applications in various sectors.

Key milestones should be clearly defined, with ambitious and technology-specific KPIs such as high yield, high-quality quantum chips, reliability, reproducibility, performance, and scalability of production. In addition, the proposal is expected to appropriately address the shortcomings identified in the Evaluation Summary Report of the corresponding FPA awarded under topic Chips-QAC-1, as appropriate to the relevant activities in the current SGA phase.

The proposal should demonstrate scalable, efficient, and stable production capabilities, with a focus on achieving high yield and consistency in quantum chip manufacturing. This will involve developing robust, repeatable manufacturing processes tailored to the unique requirements of diamond-based quantum chips, ensuring a reliable supply chain for European stakeholders. Additionally, the proposal should outline the development of reliable characterization tools to ensure quality assurance, demonstrating the scalability of pilot technologies from small-to-mid volume fabrication to large-scale industrial production. A comprehensive technology roadmap and implementation plan should be defined to guide the industrialization of quantum chip production in the future and ensure the sustainability and growth of the quantum industry.

Scope

The action will require expertise in the area of manufacturing flows for quantum technologies, in particular in quantum computing/simulation (e.g. qubit fabrication), communication and sensing, and with issues regarding high-quality, reliability, versatility, process control including integrated testing and minimizing lead times. Interaction with standardisation bodies and data sharing on benchmarking is also encouraged.

The proposal should also cover: (i) the collaboration with other initiatives or programmes at regional, national, or European level such as Framework Partnership Agreements (FPAs) awarded under topic Chips-QAC-2: Call for establishing Framework Partnership Agreement(s)

for developing Quantum Chip Technology for high-quality Stability Pilots, and the relevant Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots. This includes synergies and cooperation with the experimental pilot lines QU-PILOT and QU-TEST of the Quantum Flagship Initiative, for R&D support; (ii) any additional financial support they may receive in their activities from relevant national or regional initiatives.

In this topic the integration of the gender dimension (sex and gender analysis) in research and innovation content is not a mandatory requirement.

Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Regarding page limits:

Chapter	**FPP Phase**
Excellence	60 pages
Impact	100 pages
Quality and efficiency of the Implementation	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions:

Max Contribution per partner (% of the total EU funding): 40 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes for details).

Participation is limited to legal entities established in EU Member States, Norway, Iceland, and Israel (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled from a non-eligible country or from a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees approved by their eligible country of establishment, in so far this is a Member State or Associated Country, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Score

The scores will be given with a resolution of one decimal.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Excellence	0-5	1.0	3
Impact	0-5	1.0	3
Quality and efficiency of the Implementation	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	Maximum EU Contribution as % of the Eligible Cost according to HE (*)
For profit organization but not an SME	50 %
SME (for profit SME)	50 %
University/Other (not for profit)	50 %

(*) beneficiaries may ask for a lower contribution.

Purchases of equipment or other assets used for the action must be declared as depreciation costs. However, costs may exceptionally be declared as full capitalised costs for high-value equipment that is essential for the development of the pilots, particularly where such equipment contributes to the development of an EU ecosystem of equipment providers and users, and ultimately to European technological autonomy. This exception may apply where the equipment represents a significant share of the beneficiary's eligible costs and where limiting the cost to depreciation would introduce delays in the implementation or compromise project objectives. The list of eligible items to be declared as full capitalised costs must be part of the proposal and will be confirmed by the Chips JU during the grant preparation process.

STEP and Sovereignty Seal

This topic contributes to the objectives of the *Strategic Technologies for Europe Platform* (STEP). As such, eligible proposals that exceed the evaluation thresholds will be awarded a *Sovereignty Seal*. The Sovereignty Seal is a quality label, valid for the duration of the project, which will facilitate access to additional EU funding (alternative, cumulative or combined funding from several EU budget instruments) or national public and private investments.

3.3.5 Supporting developing Quantum Chip Technology for neutral atoms stability Pilot

Topic: HORIZON-JU-Chips-2025-QAC1-5-SGA

Type of Action	RIA Specific grant agreement in relation to a Framework Partnership Agreement
Indicative EU budget	25 M€
Expected EU contribution per project	25 M€
GMode	Co-funded with the NFA One stage, with submission of Full Project Proposal (FPP)
Invitation date	30th July 2025
Deadline FPP	17th September 2025

Context

Within the Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots, the selected consortia will be invited to submit a proposal that will implement the first 3-4 years of the action plan for providing stable pilot fabrication capabilities defined in the FPA that would foster quantum chips production and rapid innovation tailored to meet the needs of the European quantum industry over the next decade, in particular start-ups and SMEs. The testing and experimentation facilities should be fully integrated in the pilots, providing seamless production and testing services.

Expected outcomes.

The proposal should aim to establish neutral atoms stability pilot production capabilities for a first of their kind quantum technology, where in the future European companies, research centres and academic institutions can produce quantum chips on a stable pilot scale based on a shared cost model between users and service providers. The targeted stability pilot should have a simple baseline process ready in 2-3 years from start of the project - reaching at least Technology Readiness Level (TRL) 6.

An early industrialization roadmap should be available by month 6 of the project, with the expectation that it will be regularly updated throughout the project's lifetime to incorporate

evolving technical progress, market needs, and alignment with industrial partner requirements for scaling and commercialization towards mass production.

The proposal should focus on developing scalable production processes for quantum chips, with the goal of establishing industrial-level manufacturing methods. This includes the integration of cutting-edge Quantum Process Design Kits (PDKs) with the European Design Platform, aiming to standardize production workflows and minimize the need for custom developments. The proposal should include enabling technologies for quantum chips, namely advanced tools, components, and systems that facilitate the design, fabrication, operation, testing, and scaling of these devices. However, it should not include activities aimed at developing other essential components or subsystems that are unrelated or not directly integrated with the quantum chips. The initiative should seek to enhance technology and manufacturing readiness levels across the quantum industry, targeting applications in quantum computing, communications, simulations, and sensing. A key objective should be to establish standardized methodologies for the design, testing, and manufacturing of quantum chips, ensuring efficient production processes and broadening the range of applications in various sectors.

Key milestones should be clearly defined, with ambitious and technology-specific KPIs such as high yield, high-quality quantum chips, reliability, reproducibility, performance, and scalability of production. In addition, the proposal is expected to appropriately address the shortcomings identified in the Evaluation Summary Report of the corresponding FPA awarded under topic Chips-QAC-1, as appropriate to the relevant activities in the current SGA phase.

The proposal should demonstrate scalable, efficient, and stable production capabilities, with a focus on achieving high yield and consistency in quantum chip manufacturing. This will involve developing robust, repeatable manufacturing processes tailored to the unique requirements of neutral atoms quantum chips, ensuring a reliable supply chain for European stakeholders. Additionally, the proposal should outline the development of reliable characterization tools to ensure quality assurance, demonstrating the scalability of pilot technologies from small-to-mid volume fabrication to large-scale industrial production. A comprehensive technology roadmap and implementation plan should be defined to guide the industrialization of quantum chip production in the future and ensure the sustainability and growth of the quantum industry.

Scope

The action will require expertise in the area of manufacturing flows for quantum technologies, in particular in quantum computing/simulation (e.g. qubit fabrication), communication and sensing, and with issues regarding high-quality, reliability, versatility, process control including integrated testing and minimizing lead times. Interaction with standardisation bodies and data sharing on benchmarking is also encouraged.

The proposal should also cover: (i) the collaboration with other initiatives or programmes at regional, national, or European level such as Framework Partnership Agreements (FPAs) awarded under topic Chips-QAC-2: Call for establishing Framework Partnership Agreement(s)

for developing Quantum Chip Technology for high-quality Stability Pilots, and the relevant Framework Partnership Agreement (FPA) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots. This includes synergies and cooperation with the experimental pilot lines QU-PILOT and QU-TEST of the Quantum Flagship Initiative, for R&D support; (ii) any additional financial support they may receive in their activities from relevant national or regional initiatives.

In this topic the integration of the gender dimension (sex and gender analysis) in research and innovation content is not a mandatory requirement.

Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Regarding page limits:

Chapter	**FPP Phase**
Excellence	60 pages
Impact	100 pages
Quality and efficiency of the Implementation	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions:

Max Contribution per partner (% of the total EU funding): 40 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes for details).

Participation is limited to legal entities established in EU Member States, Norway, Iceland, and Israel (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled from a non-eligible country or from a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees approved by their eligible country of establishment, in so far this is a Member State or Associated Country, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Score

The scores will be given with a resolution of one decimal.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Excellence	0-5	1.0	3
Impact	0-5	1.0	3
Quality and efficiency of the Implementation	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	**Maximum EU Contribution as % of the Eligible Cost according to HE (*)**
For profit organization but not an SME	50 %
SME (for profit SME)	50 %
University/Other (not for profit)	50 %

(*) beneficiaries may ask for a lower contribution.

Purchases of equipment or other assets used for the action must be declared as depreciation costs. However, costs may exceptionally be declared as full capitalised costs for high-value equipment that is essential for the development of the pilots, particularly where such equipment contributes to the development of an EU ecosystem of equipment providers and users, and ultimately to European technological autonomy. This exception may apply where the equipment represents a significant share of the beneficiary's eligible costs and where limiting the cost to depreciation would introduce delays in the implementation or compromise project objectives. The list of eligible items to be declared as full capitalised costs must be part of the proposal and will be confirmed by the Chips JU during the grant preparation process.

STEP and Sovereignty Seal

This topic contributes to the objectives of the *Strategic Technologies for Europe Platform* (STEP). As such, eligible proposals that exceed the evaluation thresholds will be awarded a *Sovereignty Seal*. The Sovereignty Seal is a quality label, valid for the duration of the project, which will facilitate access to additional EU funding (alternative, cumulative or combined funding from several EU budget instruments) or national public and private investments.

3.3.6 Supporting developing Quantum Chip Technology for high-quality Trapped Ions Pilot

Topic: HORIZON-JU-Chips-2025-QAC2-SGA

Type of Action	RIA Specific grant agreement in relation to a Framework Partnership Agreement
Indicative EU budget	25 M€
Expected EU contribution per project	25 M€
CMode	Co-funded with the NFA One stage, with submission of Full Project Proposal (FPP)
Invitation date	30th July 2025
Deadline FPP	17th September 2025

Context

Within the Framework Partnership Agreements (FPAs) awarded under topic Chips-QAC-2: Call for establishing Framework Partnership Agreements for developing Quantum Chip for high-quality Trapped Ions Pilots, the consortium is invited to submit a proposal that will implement the first 3-4 years of the action plan for providing high-quality pilot fabrication capabilities defined in the FPA that would foster trapped-ions quantum chips production and rapid innovation tailored to meet the needs of the European quantum industry over the next decade, in particular start-ups and SMEs. The testing and experimentation facilities should be fully integrated in the pilot, providing seamless production and testing services.

Expected outcomes.

The proposal should aim to establish stability pilot production capabilities for a first of their kind quantum technology, where in the future European companies, research centres and academic institutions can produce quantum chips on a stable pilot scale based on a shared cost model between users and service providers. The targeted trapped-ions pilot should have a simple baseline process ready in 2-3 years from start of the project - reaching at least Technology Readiness Level (TRL) 6.

An early industrialization roadmap should be available by month 6 of the project, with the expectation that it will be regularly updated throughout the project's lifetime to incorporate

evolving technical progress, market needs, and alignment with industrial partner requirements for scaling and commercialization towards mass production.

The proposal should aim to develop a robust European supply chain for trapped-ion quantum technologies covering the entire value chain from materials to applications, and enhancing their availability for computing, communication, and sensing applications. The proposal should also focus on encouraging innovation within SMEs and ensuring that critical intellectual property remains within the EU. The proposal should also demonstrate high-quality production processes, emphasizing the maturation of scalable and efficient manufacturing capabilities. The integration of Quantum Process Design Kits (PDKs) should be a key focus, ensuring that the production process is streamlined and adaptable, thus enhancing Europe's leadership in quantum technologies.

The proposal should include enabling technologies for quantum chips, namely advanced tools, components, and systems that facilitate the design, fabrication, operation, testing, and scaling of these devices. However, it should not include activities aimed at developing other essential components or subsystems that are unrelated or not directly integrated with the quantum chips. By fostering a community of interest in quantum technologies and enabling the use of cutting-edge trapped-ion chips, the project will significantly boost innovation capacity, providing a competitive advantage for the European ecosystem in the global market.

Key milestones should be clearly defined, with ambitious and trapped-ion-specific KPIs such as high yield, high-quality quantum chips, reliability, reproducibility, performance, and scalability of production. In addition, the proposal is expected to appropriately address the shortcomings identified in the Evaluation Summary Report of the corresponding FPA awarded under topic Chips-QAC-2, as appropriate to the relevant activities in the current SGA phase.

Scope

The action will require expertise in the area of manufacturing flows for trapped-ion quantum technologies, in particular in quantum computing/simulation (e.g. qubit fabrication), communication and sensing, and with issues regarding high-quality, reliability, versatility, process control including integrated testing and minimizing lead times. Interaction with standardisation bodies (e.g., for trap socket designs, modularity interfaces, or photonic integration) and data sharing on benchmarking is also encouraged.

The proposal should also cover: (i) the collaboration with other initiatives or programmes at regional, national, or European level such as the Framework Partnership Agreements (FPAs) awarded under topic Chips-QAC-1: *Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilots*. This includes synergies and cooperation with the experimental pilot lines QU-PILOT and QU-TEST of the Quantum Flagship Initiative, for R&D support; (ii) any additional financial support they may receive in their activities from relevant national or regional initiatives.

In this topic the integration of the gender dimension (sex and gender analysis) in research and innovation content is not a mandatory requirement.

Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Regarding page limits:

Chapter	FPP Phase
Excellence	60 pages
Impact	100 pages
Quality and efficiency of the Implementation	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions:

Max Contribution per partner (% of the total EU funding): 40 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes for details).

Participation is limited to legal entities established in EU Member States, Norway, Iceland, and Israel (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled from a non-eligible country or from a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees approved by their eligible country of establishment, in so far this is a Member State or Associated Country, that their participation to the action would not negatively impact the Union's strategic, assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Score

The scores will be given with a resolution of one decimal.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Excellence	0-5	1.0	3
Impact	0-5	1.0	3
Quality and efficiency of the Implementation	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	**Maximum EU Contribution as % of the Eligible Cost according to HE (*)**
For profit organization but not an SME	50 %
SME (for profit SME)	50 %

University/Other (not for profit)	50 %

(*) beneficiaries may ask for a lower contribution.

Purchases of equipment or other assets used for the action must be declared as depreciation costs. However, costs may exceptionally be declared as full capitalised costs for high-value equipment that is essential for the development of the pilots, particularly where such equipment contributes to the development of an EU ecosystem of equipment providers and users, and ultimately to European technological autonomy. This exception may apply where the equipment represents a significant share of the beneficiary's eligible costs and where limiting the cost to depreciation would introduce delays in the implementation or compromise project objectives. The list of eligible items to be declared as full capitalised costs must be part of the proposal and will be confirmed by the Chips JU during the grant preparation process.

STEP and Sovereignty Seal

This topic contributes to the objectives of the *Strategic Technologies for Europe Platform* (STEP). As such, eligible proposals that exceed the evaluation thresholds will be awarded a *Sovereignty Seal*. The Sovereignty Seal is a quality label, valid for the duration of the project, which will facilitate access to additional EU funding (alternative, cumulative or combined funding from several EU budget instruments) or national public and private investments.

3.4 Lab to Fab Accelerators Ecosystem

With its rapidly rising computing demands, Europe's vibrant industrial ecosystem needs new perspectives for a substantial growth potential. Using traditional monolithic SoCs, design and fabrication costs are increasing exponentially from one leading edge node to the next. Chiplets, instead, can be an efficient and economical way out providing the basis for a crucial push. Using chiplets in packaging architectures aims to reduce product costs while enabling the manufacture of new high-performance functionalities.

With their modular design, chiplet architectures allow the mix-and-match of various functional blocks, thus providing greater flexibility and making it easier to customise and upgrade computing components, driving scalability and adaptability. This way, they meet the demands of industrial sectors like high-performance computing, automotive, avionics, aerospace, communications, and secure & trustworthy electronics systems.

However, a successful integration of chiplets requires advanced heterogeneous integration techniques. Surpassing traditional methods like full-chip integration and 2.5D integration, they will pave the way for emerging innovative chiplet business models potentially reshaping market segments in the coming years. While the benefits of this evolution for the European economy appear to be obvious, the success of this transition will largely depend on targeted transfer activities from the lab into European fabs – for an optimised exploitation right from the pilot line to the industry.

To that end, the European Union is funding the establishment of European RTO-based pilot lines addressing innovative and advanced packaging technologies. Notably, the APECS pilot line, which unites leading research institutes across Europe in advanced packaging, the NanoIC pilot line offering advanced interconnect technologies, the FAMES pilot lines with new 3D integration options, as well as the PIXEurope and WBG pilot lines, which focus on the integration and packaging of photonic and high-power integrated circuits.

These pilot lines implemented under the EU Chips Act, will serve as key research providers for latest heterogeneous integration and advanced packaging technologies.

To achieve the effective incorporation of heterogeneously integrated and chiplet-based systems and establish a seamless pipeline from research to product development to pilot lines, Lab to Fab Transfer Accelerator (LFA) projects will be crucial for a rapid take-up of these technologies by European industry.

3.4.1 Lab to Fab Accelerators for Advanced Packaging and heterogeneous integration

Topic: DIGITAL-JU-Chips-2025-SG-LFA

Type of Action	Simple Grant
Indicative EU budget	50 M€
Expected EU contribution per project	The JU estimates that an EU contribution between EUR 12 and 16 million per project would allow to appropriately address the expected outcomes. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Co-funded with the NFA One stage Call, with submission of Full Project Proposal (FPP)
Call launch date	3 December 2025
Deadline FPP	07 May 2026 at 17:00 Brussels Time

Context

The Lab-to-Fab Transfer Accelerator (LFA) projects prepare for a faster take-up of latest packaging technologies by the European industry. They do not cover the full lab-to-fab trajectory but prepare it and should enable a seamless fab technology transfer to industry after the end of the project.

Expected outcomes.

This topic will open up new opportunities for European-based semiconductor packaging companies and their supply chain by building on currently available services of RTOs and all Chips JU pilot lines. The LFA projects should prepare and speed up the transfer of technologies from pilot lines to industrial deployment.

In addition, projects should expand the advanced packaging ecosystem in Europe and boost its competitiveness by offering a fast path towards industrialization of European semiconductor technology.

Through possible involvement of appropriate actors across the value chain – from materials, substrate, equipment, and test providers through packaging companies and their European customers – proposed projects should build a strong European innovation and transfer

ecosystem for advanced packaging solutions, contributing to new and resilient supply chains in Europe.

Project proposals need to address several of the following expected outcomes:

- **Advanced packaging solutions tailored to European market needs** available for direct transfer into mass manufacturing within European production facilities (TRL 7) establishing a foundation for large-scale production in Europe for targeted application sectors.
- **Optimized utilization and demonstrable impact of Chips JU pilot lines**, accelerating development and validation of advanced packaging innovations.
- **Enhanced global competitiveness of European industry**, through increased capabilities in advanced packaging technologies (including chiplets), supporting faster adoption of cutting-edge semiconductor technologies in Europe.
- **Lowered economic and technical barriers for industrial capacity expansion**, through co-development enabling quicker adoption of heterogeneous integration and chiplet technologies in commercial products.
- **Strengthened investment confidence and market traction** for medium- to high-volume production by proving the readiness of technologies for qualified series manufacturing.
- **Alignment of advanced packaging capabilities in Europe with needs in strategic application areas**, including edge high-performance computing (eHPC), artificial intelligence (AI), power electronics, sensors, photonics, security, safety, and mobility.
- **Improved electronic system performance and energy efficiency**, achieved through integration of multichip, chiplet, and 3D technologies in high-demand applications such as eHPC, AI, and 5G.
- **Contribution to environmental sustainability and resource efficiency**, through advanced module and package designs that reduce material and energy usage in chip production.

Scope

To bring the latest advanced packaging technologies from the Chips JU pilot lines to industrial advanced packaging sites across Europe faster, the Chips Joint Undertaking will support **pan-European technology transfer preparation projects** to accelerate the post-project transfer from Chips JU pilot lines into key application domains.

The focus of the proposed projects should be on joint development, led by industry, of the most advanced packaging technologies with the Pilot lines to enable a future transfer of the latest packaging technologies from pilot lines into industrial production sites. The proposed projects are expected to cover the necessary value chain steps up to manufacturing, and develop industrial-grade, high-yield advanced packaging technologies including process developments up to TRL 7.

The proposed projects should define pathways into (one of) the following **two industrialization streams after the end of the projects**:

(1) Enabling an open-access heterogeneous integration and chiplet packaging **foundry** for European key applications;

(2) and/or **transfer of technologies** to companies for setting-up or upgrading own advanced packaging manufacturing lines **in Europe** for key European markets.

Proposal consortia should be led by industry and contain concrete deployment scenarios for one or both of those streams.

The proposed projects should address one or more of the following topics:

1) Special demands for **Communication Technologies** and **RF based applications**, e.g.
   - WLP and Fan-Out Wafer Level Packaging (FOWLP) with RDL for small and medium volume;
   - Efficient heterogeneous integration strategies of multiple material systems, e.g. Si, GaN, GaAs and 2D materials;
   - Special requirements of high frequency radars especially for the interconnection between the components and the substrate to guarantee the high performance of the whole system;
   - Other RF specific packaging needs not covered above.
2) Special demands for **Photonics applications**, e.g.
   - Optical Die-to-Die communication packaging solutions;
   - Co-packaging of photonics for known-good tested Photonic ICs;
   - Standardisation of optical die interface to facilitate automatic testing operations;
   - Efficient heterogeneous integration strategies of multiple material systems, e.g. Si, SOI, SiN, InP, and 2D materials;
   - Other photonics specific packaging needs not covered above.
3) Special demands for **HPC, edge-HPC and power delivery**, e.g.
   - Advanced and highly functional organic IC substrates with a 4× reduction in line/space and pad pitch, achieving feature dimensions comparable to those of silicon interposers and silicon bridges;
   - Introduction of novel materials, such as glass, for advanced IC substrates enabling enhanced functional integration, including embedded components;
   - Adherence to application-specific packaging guidelines, e.g. Large Package for HPC and AI (e.g. IC-substrate CTE and materials);
   - Integrated passive/active devices manufacturing in RDLs and substrates;
   - 3D interconnect methods including hybrid bonding;
   - Packaging and cooling of high-power-dissipating components/modules including smart power chips and PMICs (e.g. embedding);
   - Other HPC and edge-HPC specific packaging needs not covered above including integration of new functionalities, devices and packaging technologies.
4) Special demands for **Novel Sensor Applications**, e.g.

- Advanced packaging, 3D integration and WLP for sensors and actuators;
- Embedded active devices / components / novel sensor and actuator approaches (like TMR and others) in PCB/IC-substrate with chip(s) assembly co-design, leveraging the Design Platform capabilities;
- MEMS test and simulation including stress sensor for calibration and chip-package interaction and in-field compensation;
- Higher system integration level for ECUs and sensors/actuator modules:
  - Logic + Memory (computing/embedded HPC);
  - Logic + Power + Sensor + Actuator integration.
- Other novel sensors specific packaging needs not covered above.

5) Special demands for **automotive, and other harsh environment applications** (such as energy, industrial, avionics, aerospace, etc.), e.g.
   - Parts, materials and processes for extreme application (exceeding -55 / +125°C) such as GaN, SiC, Diamond related semiconductors;
   - Development of packaging and assembly procedures for very high temperature applications including high power and thermal control;
   - Assessment of new materials for very high radiation dose;
   - Development of new testing procedures for very extreme temperatures (i.e. sockets, thermal chambers, feedthrough connectors, etc.);
   - Other harsh environments specific packaging needs not covered above.

In addition, accelerator projects should enable a faster qualification and technology transfer of advanced packaging and heterogeneous chip integration technologies for uptake by European manufacturing sites. More specifically, the proposed projects should:

- **Address industrial requirements** for advanced heterogeneous integration and chiplet based future products regarding cost, performance, security and reliability standards.
- **Pave the way to manufacturability** by manufacturing-grade process developments and standardisation for scalability and cost competitiveness.
- **Include implementation Roadmap**: Proposals should provide an implementation roadmap for enabling Chips Act related first-of-a-kind investments in Europe that address industrialisation and technology expectations beyond the project's duration and capacity.
- **Design for built-in testability**, i.e. cooperation with chiplet designers to ensure that chiplets will be accessible for testing by Automatic Test Equipment.
- **Enhance faster industrial technology qualification schemes and adaptation** with qualification plans for appropriate verticals with suitable reliability tests for market and mission profile, enabling fast track to industrial deployment.
- **Apply "System Technology Co-Optimization" (STCO)**, address increased modularity and reusability of design blocks and enhance standardized integration technologies based on PDKs (process design kits) and ADKs (assembly design kits) for the heterogeneous chiplet packaging.
- **Address EDA verification**, i.e. design rule checks, process design checks.

- **Utilize advanced materials**, e.g. advanced substrates including organic but also inorganic ones, i.e. glass technologies.

All projects selected from this call are expected to contribute actively to the CSA, under the topic DIGITAL-Chips-2025-CSA-LFA, that will support the projects selected under this topic and that will coordinate core efforts to ensure a coherent ecosystem development, standardisation tasks and cross-sectional technology exchange to create maximum synergies.

Admissibility

Admissibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Regarding page limits:

Chapter	FPP Phase
Relevance	60 pages
Implementation + chapter 4 of the template for the proposal (Part B)	100 pages
Impact	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

Eligibility

Eligibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Specific eligibility conditions:

Size limit	15 participants
Max EU Contribution per partner (% of the total EU funding)	50%

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to participation restrictions for the protection of European digital infrastructures, communication and information systems, and related supply chains, as described in Annex 4 of the WP General Annexes.

Legal entities that are established in the Union or EEA countries but are controlled from third countries may only participate on the condition that they guarantee the protection of the essential security interests of the Union and the Member States and that they ensure the protection of classified documents information. Where applicable, security guarantees need to be provided after proposal selection.

Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Evaluation procedure

For the specificity of each call evaluation please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

For the priority order of proposals with the same score, please refer to Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Award criteria.

Please refer to Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Specific rules may apply regarding the eligibility to national funding.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Score

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Relevance	0-5	1.0	3
Implementation + chapter 4 of the template for the proposal (Part B)	0-5	1.0	3
Impact	0-5	1.5	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to DIGITAL.

Type of beneficiary	EU Contribution as % of the Eligible Cost according to DIGITAL (*)
For profit organization but not an SME	25 %
SME (for profit SME)	35 %
University/Other (not for profit)	35 %

(*) beneficiaries may ask for a lower contribution.

3.4.2 Lab to Fab Accelerator ecosystem - Coordination and Support Actions. Boosting cooperation for industrial implementation on advanced packaging of chiplets and heterogeneous integration in Europe.

Topic: DIGITAL-JU-Chips-2025-CSA-LFA

Type of Action	Coordination and Support Actions (CSA)
Indicative EU budget	2 M€
Expected EU contribution per project	The JU estimates that an EU contribution of around EUR 2 million would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amount.
Mode	EU funding only One stage Call with submission of Full Project Proposal (FPP)
Call launch date	03 December 2025
Deadline FPP	07 May 2026 at 17:00 Brussels Time

Context

This coordination and support action will support the Lab to Fab Transfer Accelerator (LFA) projects to leverage synergies and standardisation efforts, maximising the efficiency of joint deployment and speeding up future transfer into industrial applications. It will help to close gaps in advanced packaging capabilities in Europe and contribute to building a stronger European ecosystem.

Therefore, this CSA is intended to effectively support the **selected projects under Call DIGITAL-JU-Chips-2025-SG-LFA**.

Expected outcomes.

This CSA is expected to deliver a more resilient, sustainable, and competitive European advanced packaging ecosystem through focused collaboration, standardization, and workforce development.

The following outcomes are expected:

1. Resilient & Diversified Supply Chains (Addressing Supply Network Ecosystems)

A demonstrably more resilient European supply chain for advanced packaging, evidenced by a publicly available vulnerability assessment for key sectors (automotive, aerospace, healthcare, security, telecommunications).

2. Sustainable & Resource-Efficient Manufacturing

Reduced environmental footprint of advanced packaging manufacturing in Europe, demonstrated by measurable improvements in resource consumption (materials, energy) and adoption of sustainable design principles.

3. Accelerated Standardization & Interoperability

Increased adoption of standardized technologies for advanced packaging, fostering interoperability and reducing time-to-market for European companies.

4. Enhanced Collaboration & Knowledge Sharing

A strengthened and interconnected European advanced packaging ecosystem, characterized by increased collaboration between research institutions, industry, pilot lines, competence centres, and existing networks (e.g. Pack4EU).

5. Coordinated R&I & Industrial Implementation

A harmonized roadmap for the industrial implementation of research results in advanced packaging, ensuring coherence between EU R&I activities and industry needs.

6. Skilled & Competent Workforce

A skilled workforce equipped to support the growth of the European advanced packaging ecosystem, with increased availability of specialized training programs and upskilling opportunities.

Scope

The CSA should address, but is not limited to, the following areas:

Enable **collaboration and exchange**:

- Provide coordination on common objectives and coordinated dissemination between the projects of the LFA programme,
- Disseminate to and between lab-to-fab projects best practices in “System Technology Co-Optimization” (STCO) and support building STCO ecosystems at project level,
- Organise networking and collaboration of stakeholders from the EU with a view to addressing current needs, considering future requirements and stimulating long-term cooperation,
- Connect with and leverage services by competence centres to derive training material and platform information, serving competence centres, pilot lines and the design platform,
- Foster the exchange of achievements in Process Design Kit (PDK) and Assembly Design Kit (ADK) for the heterogeneous chiplet packaging, and the EDA verification.

Identifying, mapping and disseminating of **standardisation** results:

- Support standardised integration technologies based on PDKs (process design kits) and ADKs (assembly design kits), complementing the offering of the Pilot lines' PDKs,
- Monitor manufacturing-grade process developments and standardisation for scalability and cost competitiveness,
- Track heterogeneous package integration schemes that are customisable and flexible, to enable diversified advanced packaging building blocks for European markets,
- Collect and disseminate the project results on standardised or exchangeable interfaces for all packaging layers, e.g. for chiplet and other advanced semiconductor-based components,
- Foster and report on intelligent leveraging and developing technological standards to provide credible cost-down pathways and competitive time-to-market.

Identify and support **roadmap activities and synergies**:

- Organise and support roadmap activities
    - through networks, conferences, workshops and other actions that support semiconductor joint EU R&I activities,
    - by generating R&I priorities for potential future collaboration,
    - by connecting EU companies in the semiconductor value chain to exchange information and propose measures to improve chip supply chain stability.
- Support exchange of researchers and closer coordination of running R&I activities which address equal or similar objectivities to leverage synergies,
- The action should ensure that relevant stakeholders from the EU are engaged during the process through regional and international workshops and a set of communication and dissemination actions.

Reminding that of general importance to the Chips JU calls are:

- Re-use of results from previous ECSEL JU, Chips JU, H2020, HE or EUREKA-cluster projects on the Packaging topic is encouraged. Of particular importance the CSA is expected to build up on the results of the Pack4EU CSA.
- Developing synergies with other relevant European, national or regional initiatives and/or funding programmes on the Packaging topic.
- Collaboration with industrial associations in the field (e.g. with EPoSS and AENEAS) and specialized clusters. Collaboration with associations of microelectronic assembly and packaging science.
- In particular, paying attention to the needs of SMEs, involving SMEs, start-ups and scale-ups in project execution, and develop solutions that can be taken up and/or exploited by SMEs.

To ensure proper coordination and support to the LFA programme, the CSA is expected to have a 4-year duration.

Admissibility

Admissibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Regarding page limits:

Chapter	FPP Phase
Relevance	20 pages
Implementation + chapter 4 of the template for the proposal (Part B)	60 pages
Impact	20 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

Eligibility

Eligibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Specific eligibility conditions:

Size limit	15 participants
Max EU Contribution per partner (% of the total EU funding)	50%

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to participation restrictions for the protection of European digital infrastructures, communication and information systems, and related supply chains, as described in Annex 4 of the WP General Annexes.

Legal entities that are established in the Union or EEA countries but are controlled from third countries may only participate on the condition that they guarantee the protection of the essential security interests of the Union and the Member States and that they ensure the protection of classified documents information. Where applicable, security guarantees need to be provided after proposal selection.

Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Evaluation procedure

For the specificity of each call evaluation please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

For the priority order of proposals with the same score, please refer to Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Award criteria.

Please refer to Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Specific rules may apply regarding the eligibility to national funding.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

Score

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Relevance	0-5	1.0	3
Implementation + chapter 4 of the template for the proposal (Part B)	0-5	1.0	3
Impact	0-5	1.0	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to DIGITAL.

Type of beneficiary	EU Contribution as % of the Eligible Cost according to DIGITAL (*)
For profit organization but not an SME	100 %
SME (for profit SME)	100 %

University/Other (not for profit)	100 %

(*) beneficiaries may ask for a lower contribution.

4 ANNEX: COUNTRY SPECIFIC ELIGIBILITY RULES FOR INITIATIVE CALLS 2025

The conditions and rules expressed in the next Participating State' sections apply only to the participants of that Participating State in particular as to their eligibility for national funding or as to the attribution of national funding.

Austria

National contact person for Chips JU programme

Country	Name	First name	Tel	E-mail
AUSTRIA	Hartmann	Olaf	+43 (0)5 7755 4902	olaf.Hartmann@ffg.at
AUSTRIA	Ristanic	Daniela	+43 (0)5 7755-5137	daniela.ristanic@ffg.at

National Funding Agency for Austria: FFG

The full version of the national eligibility criteria can be found at the national homepage of the Call www.ffg.at/chips/as2025.

Legal requirements for the eligibility of a partner or a project

Type or nature of participants

Legal entities, partnerships and sole traders that are not part of the Austrian federal administration are eligible to receive funding.

The following are eligible for funding:

- Companies of any legal form
- Institutions of research and knowledge dissemination
  - Universities[24]
  - Universities of applied sciences
  - Non-university research institutions
  - Technology transfer institutions, innovation agents and other research-oriented organisations such as associations with a relevant purpose
- Other non-commercial institutions
  - Local authorities and autonomous bodies (Note: Activities of local authorities falling within

[24] The smallest possible unit of a university is an institute of the university or a organisation comparable to a UOG 2002/§20 organisation unit. It is a precondition that the participating organisation unit (institute or comparable unit) is authorised with corresponding mandate according to UOG 2002/§ 27. Units below (for example working groups) can not act as project partners.

- their statutory mandate are not eligible for funding)
- Non-profit making organisations such as NPOs("Non-profit making organisations" do not distribute profits to their owners, members or other natural persons or legal entities in accordance with their legal status or articles of association.)

Legal, administrative, and financial conditions

The national application of Austrian partners has to be submitted electronically via eCall before the deadline of the project submission.

Formal correctness and completeness of the application are examined in a formal check.

FFG experts will check the financial viability (credit rating and liquidity) of the participating enterprises. It is not possible to provide funding to undertakings in difficulty (as defined in the General Block Exemption Regulation (OJ L 187/19 in its current version, Art. 2 subpar. 18). Austrian enterprises have to provide the following documents:

- Annual statement of accounts (balance sheet, profit and loss account) from the past 2 financial years;
- Declaration of SME Status for associations and sole traders
- The company size is to be determined according to the SME definition as specified by EU competition law: information on SME definition.

Criteria on project composition for the Austrian participants

The ratio of the personnel resources (persons*months allocated) between Austrian companies and Austrian research organisations has to be 1.5 to 1 or higher within each project bundle in the national contract preparation phase and throughout the entire project duration. All national submissions belonging to the same transnational (Chips JU) project are considered as a project bundle.

Other conditions

Under ECS Call the following Topics are eligible for national funding in the research category of experimental development:

- **HORIZON-JU-Chips-2025-IA:** Global call according to SRIA 2024 (IA)
- **HORIZON-JU-Chips-2025-IA FT1:** Focus topic on "RISC-V Automotive Hardware Platform"
- **HORIZON-JU-Chips-2025-IA FT2:** Focus topic on "AI-assisted Methods and Tools for Engineering Automation"

The following Topic is eligible for national funding in the research category of industrial research:

- **HORIZON-JU-Chips-2025-RIA**: Global RIA call

Under the Chips for Europe Initiative the following Topic is eligible for national funding in the research category of experimental development:

HORIZON-JU-Chips-2025-IA-EDA: Call on Open-source EDA tools development

The planned distribution of the national budget to the different topics is outlined below:

Table 1 Budgetaufteilung (Indikative Werte) - Call 2025-1(IA)

Call 2025-1 (IA)	National Budget
HORIZON-JU-Chips-2025-IA **Global call according to SRIA 2024 (IA)**	3.0 Mio. EUR
HORIZON-JU-Chips-2025-IA FT1 **Focus topic on "RISC-V Automotive Hardware Platform"**	2.0 Mio. EUR
HORIZON-JU-Chips-2025-IA FT2 **Focus topic on "AI-assisted Methods and Tools for Software-Defined Vehicle Engineering Automation"**	1.4 Mio. EUR

Table 2 Budgetaufteilung (Indikative Werte) - Call 2025-1(RIA)

Call 2025-1 (RIA)	National Budget
HORIZON-JU-Chips-2025-RIA **Global call according to SRIA 2025 (RIA)**	3.6 Mio. EUR

Table 3 Budgetaufteilung (Indikative Werte) - Open-source EDA tools development

Open-source EDA tools development	National Budget
HORIZON-JU-Chips-2025-IA-EDA	0.5 Mio. EUR

Austria aims to reach a good balance between hardware-oriented projects and software oriented projects. Furthermore, the objective of the national funding programme is to prioritise projects that demonstrate a compelling impact in Austria, particularly those that strengthen the Austrian research and Industrial community in the field of Electronics and Software based Systems (see e.g. Technical Position Paper 2023 of the ESBS-Austria Association). Applicants are requested to take into consideration the total national commitment per topic (available national funding budget) when defining their participation in this Call. In order to support a reasonable balance in the distribution of national funding, single organisations should avoid applying for an excessive total national funding amount. Project participations of Austrian partners are eligible for national funding only if they comprise mainly R&D activities.

Eligibility of the costs and funding

Eligibility of costs

The eligibility of costs is in accordance with the national rules on eligible costs. For details on the eligibility of costs, see the Cost Guidelines Version 3.1. Eligible costs must be allocable directly to the project. This means that:

- they are incurred additionally to the normal operating costs during the funding period
- they are in accordance with the Funding Contract
- they can be evidenced by receipts or other type of valid documentation (e.g. timesheets, equipment use records, etc.)

Non-deductible value added tax paid by the beneficiary which is not refunded according to national legislation is eligible. The earliest possible date for the start of the project is after submission of the application for funding.

Funding rates

The maximum funding rates depend on the research category, the type and size of organisation and the call topic.

Percentage of the national subsidy to the beneficiaries

Table 4: Maximum funding rates

Research Category	Call and Topic8	Large enterprise	Medium-sized enterprise	Small enterprise	Research institutions and other institutions (non-commercial activities)
Experimental development	**HORIZON-JU-Chips-2025-IA** Global call according to SRIA 2024 (IA)	up to 20 %	up to 20 %	up to 30 %	up to 30 %
Experimental development	**HORIZON- Chips-2025-IA FT1**	up to 15 %	up to 15 %	up to 25 %	up to 30 %
Experimental development	**HORIZON-JU-Chips-2025-IA FT2**	up to 15 %	up to 15 %	up to 25 %	up to 30 %
Industrial Research	**HORIZON-JU-Chips-2025-RIA** Global RIA call	up to 25 %	up to 35 %	up to 40 %	up to 35 %
Experimental development	**HORIZON-JU-Chips-2025-IA-EDA**	up to 15 %	up to 20 %	up to 30 %	up to 30 %

To determine the company size see information on SME Definition. In addition, the following needs to be considered:

- If the contributions to the project involve a commercial activity, the funding rates for research institutions and other institutions are the same as those for enterprises.

- The centre of gravity of individual Austrian partner's project participation has to be within the type of action that the overall project addresses (RIA/IA).
- Experimental development does not extend beyond the system completion and validation (TRL 8). Exception: commercially usable prototypes and pilot projects, if the developed product would be too expensive for demonstration and validation purposes alone.

Additional Information to be provided at submission and other conditions.

- Registration (national submission) at the eCall System
- Completion of all relevant forms
- Upload of relevant documents in the eCall: balance sheets, **"Chips 2025 Project Contribution for Austrian partners"**, etc.

National Guidelines And Eligibility Criteria For Austrian Participants In The Call Lab To Fab Accelerators For Advanced Packaging And Heterogeneous Integration

Legal requirements for the eligibility of a partner or a project

Type or nature of participants

Only Austrian participants who are listed as partners in the transnational consortium(s), that has(have) been selected for funding from the Chips Joint Undertaking and who are beneficiaries in the respective Simple Grant Agreement(s) with the Chips JU are eligible for national funding.

Legal entities, partnerships and sole traders that are not part of the Austrian federal administration are eligible to receive funding.

The following are eligible for funding:

- Companies of any legal form − Institutions of research and knowledge dissemination
  - Universities[25]
  - Universities of applied sciences
  - Non-university research institution
  - Technology transfer institutions, innovation agents and other research oriented organisations such as associations with a relevant purpose
- Other non-commercial institutions
- Local authorities and autonomous bodies (Note: Activities of local authorities falling within their statutory mandate are not eligible for funding)

[25] The smallest possible unit of a university is an institute of the university or an organisation comparable to a UOG 2002/§20 organisation unit. It is a precondition that the participating organisation unit (institute or comparable unit) is authorised with corresponding mandate according to UOG 2002/§ 27. Units below this size (for example working groups) cannot act as project partners.

- Non-profit making organisations such as NPOs ("Non-profit making organisations" do not distribute profits to their owners, members or other natural persons or legal entities in accordance with their legal status or articles of association.)

Legal, administrative and financial conditions (Submission Procedure)

The national application of Austrian partners has to be submitted electronically via eCall before the deadline of the project submission.

Formal correctness and completeness of the application are examined in a formal check.

FFG experts will check the financial viability (credit rating and liquidity) of the participating enterprises. It is not possible to provide funding to undertakings in difficulty (as defined in the General Block Exemption Regulation (OJ L 187/19 in its current version, Art. 2 subpar. 18). Austrian enterprises have to provide the following documents:

- Annual statement of accounts (balance sheet, profit and loss account) from the past 2 financial years
- Declaration of SME Status for associations and sole traders
- The company size is to be determined according to the SME definition as specified by EU competition law: information on SME definition.

Project composition for the Austrian participants

The ratio of the personnel resources (persons*months allocated) between Austrian companies and Austrian research organisations has to be 1,5 to 1 or higher within each project bundle in the national contract preparation phase and throughout the entire project duration. All national submissions belonging to the same transnational (Chips JU) project are considered as a project bundle.

Other conditions

The focus of the proposed overall JU projects should be on experimental development, led by industry, of the most advanced packaging technologies with the Pilot lines to enable a future transfer of the latest packaging technologies from pilot lines into industrial production sites. The proposed projects are expected to cover the necessary value chain steps up to manufacturing, and develop industrial-grade, high-yield advanced packaging technologies including process developments up to TRL 7.

Applicants are requested to take into consideration the total national commitment per call (available national funding budget) when defining their participation. Project participations of Austrian partners are eligible for national funding only if they comprise mainly R&D activities (e.g. partners solely pursuing project management activities are not eligible).

Eligibility of costs and funding

Eligibility of costs

The eligibility of costs is in accordance with the national rules on eligible costs. For details on the eligibility of costs, see the Cost Guidelines Version 3.2. Eligible costs must be allocable directly to the project. This means that:

- they are incurred additionally to the normal operating costs during the funding period
- they are in accordance with the Funding Contract
- they can be evidenced by receipts or other type of valid documentation (e.g. timesheets, equipment use records, etc.)

Non-deductible value added tax paid by the beneficiary which is not refunded according to national legislation is eligible.

The earliest possible date for the start of the project is after submission of the application for funding.

Funding rates

The maximum funding rates depends on the research category and on the type and size of organisation.

Percentage of the national subsidy to the beneficiaries based on the eligible cost

Table 1: Maximum funding rates

Research Category	Large enterprise	Medium-sized enterprise	Small enterprise	Research institutions and other institutions (non-commercial activities)
Experimental development	up to 15 %	up to 15 %	up to 25 %	up to 35 %

To determine the company size, see information on SME Definition.

In addition, the following needs to be considered:

- If the contributions to the project involve a commercial activity, the funding rates for research institutions and other institutions are the same as those for enterprises.
- The centre of gravity of individual Austrian partner's project participation has to be within the type of action that the overall project (here: Experimental development).
- Experimental development does not extend beyond the system completion and validation (TRL 8). Exception: commercially usable prototypes and pilot projects, if the developed product would be too expensive for demonstration and validation purposes alone.

The instalment plan for the payment of the funding and the respective reporting periods are aligned with the specifications in the European Grant Agreement, as long as they are not contradicting national regulations.

Additional information to be provided at submission and other conditions

- Registration (national submission) at the eCall System;
- Completion of all relevant forms;
- Upload of relevant documents in the eCall: balance sheets, “Chips 2026 Project Contribution for Austrian partners”, etc.

Belgium

National contact person for Chips JU programme

Country	Name	First name	Tel	E-mail
BELGIUM				
Flanders	DEPREZ	Francis	+32 494 589672 +32 2 432 4301	francis.deprez@vlaio.be
	MONTE	Ann	+32 473 363600 +32 2 432 4207	ann.monte@vlaio.be
Brussels-Capital Region	MAAS	Stijn	+32 2 600 5067	smaas@innoviris.brussels
Wallonia	MORANA	Cedric	+32 81 33 45 37	cedric.morana@spw.wallonie.be

Funding authority websites: Flanders: www.vlaio.be
Brussels: www.innoviris.brussels
Wallonia : www.recherche.wallonie.be

Additional for Chips JU (Flanders):

- www.vlaio.be Chips JU specific pages
- https://www.vlaio.be/nl/subsidies-financiering/subsidies-voor-ooi-een-internationaal-consortium/netwerken/chips-ju-chips-joint-undertaking Chips JU specific pages

Legal requirements for the eligibility of a partner or a project

1) Type or nature of participants

For Flanders:
The participant must be a company established in Belgium, with a sustainable economic activity in Flanders, based upon a sound business model.
Flemish Strategic Research Centres (SOC) can be independent legitimate participants.
Research centres and universities can only be legitimate participants in projects compliant to the Flemish O&O-subsidy conditions (Research Partner)
For Brussels:
Participants in CHIPS JU projects wishing to receive funding from Innoviris must be companies, universities or research organisations (in accordance with the definitions provided

for by the General Block exemption Regulation for State Aid and the Brussels legislation regulating the action of Innoviris) established on the territory of the Brussels-Capital Region and performing RDI activities within the project.
Please note that no individual partner alone is allowed to support more than 70% of the project's cost.

For Wallonia:

Participants in CHIPS JU projects must be companies, universities/Colleges or accredited research centres established in the Walloon Region and performing RDI activities within the project.

2) Legal, administrative and financial conditions

For Flanders:

Any double public funding of activities is prohibited.
In case of a multinational company, the application needs to be done by the Belgian legal entity or subsidiary.
For the independent project participation of a research centre or university, the legitimate status of Strategic Research Centre (SOC) is mandatory. A specific agreement with VLAIO is compulsory and Flemish governmental funding outside "Fonds voor Innoveren en Ondernemen" applies.
For enterprises "State Aid for Rescuing and Restructuring Firms in Difficulty" is applicable, according Europea definitions (holding level).

For Brussels:

For Brussels enterprises wishing to benefit from Innoviris funding, the financing conditions are as follows:

- develop all or some of its R&D activities within the territory covered by the Brussels-Capital Region
- present an innovative RDI project likely to have a favourable impact on employment and/or sustainable development of the Brussels-Capital Region
- show one's ability to finance one's share in the project
- the company is not in difficulty, in accordance with the European legislation
- have fulfilled its obligations in the context of previous support initiatives allocated by the Region.

No other public funding (except the European contribution provided by the JU) can be received by the beneficiaries for the activities performed within the project. Any other funding must be declared to Innoviris.

For Wallonia:

The Walloon decree on RDI support (25/06/2008) is the Walloon legal basis to determine the funding of the participants. Participants must be based in Wallonia and the Walloon company(ies) must have a business unit in Wallonia.
The companies have to present an innovative RDI project with a favourable impact on the Walloon economy and/or in terms of employment in alignment with the Walloon S3, as well on sustainable development in Wallonia.

The participants cannot benefit from any other public funding for the same activities.
The participants have fulfilled their obligations in the context of previous support allocated by the Region.
The companies in difficulty, in accordance with the European legislation, cannot not be funded.

3) Consortium configuration

For Flanders:
Project application is done by either an enterprise with a legal entity in Belgium and effective operations in Flanders or a legitimate Strategic Research Centre.
Project participation needs to be primarily executed to the benefit of the applying entities.
Participation of research organisations is only possible as research partner (legal subcontracting) to the participation of an enterprise with co-funding by the enterprise.
Applications compliant to the status of Strategic Research Centre need to be done independently.
For Brussels:
Participants in CHIPS JU projects wishing to receive funding from Innoviris must be a company or a research organisation.
For Wallonia:
The Walloon partners of the consortium must include at least one company and the research budget of the Walloon partner company(ies) must correspond to at least 40% of the total budget of all Walloon partners.

4) Other conditions

For Flanders:
Enterprises need to prove adequate (financial) means to execute the project and a potential to use the results.
The project should yield socio-economic effects which can be quantified by activities or investments after the completion of the project, by exploitation in Flanders based entities, in accordance with the ruling detailed in the document (except for project applications by Strategic Research Centres). Conditions are compliant to the impact conditions of O&O, detailed on:
www.vlaio.be/nl/subsidies-financiering/onderzoeksproject/voorwaarden-om-aanmerking-te-komen-voor-de-subsidie (RIA-projects)
www.vlaio.be/nl/subsidies-financiering/ontwikkelingsproject/wie-komt-aanmerking-en-onder-welke-voorwaarden (IA-projects)
Project qualification ‘research’ or ‘development’ will follow Chips JU call rationale (IA, RIA or additional calls).
In case of potential military applications (including dual use), funding can be restricted.
For Brussels:
Exploitation and valorisation conditions:
Brussels-based participants must demonstrate their capability to carry out the tasks assigned to them in the project, exploit the results of the latter and the project's likelihood to have a positive

impact on the Brussels-Capital Region from a social, environmental and the regional ecosystem perspective 's (economy, employment, and/or sustainable development, inequalities, working conditions, well-being, …).
In case of potential military applications (including dual use), funding can be restricted.
For Wallonia:
The participants must demonstrate their capability to carry out the tasks assigned to them in the project, exploit the results of the latter and have positive impacts on Wallonia from a socio-economic and sustainable development perspective.
Projects must be targeted at civilian technologies, products, processes and services only.

5) Eligibility of costs

For Flanders
Eligibility of costs is in accordance with the ruling of the O&O bedrijfssteun of Flanders, detailed in the documents available on:
https://www.vlaio.be/nl/subsidies-financiering/onderzoeksproject/welk-bedrag-kan-je-krijgen-de-subsidie-onderzoeksproject
www.vlaio.be/nl/subsidies-financiering/ontwikkelingsproject/financiele-steun-voor-een-ontwikkelingsproject
Eligible cost calculation will be done on the costs formulated in the CHIPS JU application. The cost model applicable is the Chips JU eligible cost system (Horizon Europe)
In case of stand-alone Strategic Research Centre projects, CHIPS JU eligible cost system (Horizon Europe) is applicable for both Chips JU and SOC funding.

For Brussels
For Chips JU projects, the Brussels-Capital Region will align on the JU and will therefore not apply additional rules, such as the regional rules applicable for individual RDI projects, on the eligibility of costs. The eligible costs will therefore be those retained by the JU for the European contributions in accordance with the Horizon Europe Rules for Participation.

For Wallonia:
The eligibility of costs is in accordance with the guidelines issued by the Public Service of Wallonia available on:
Guide-des-dépenses-admissibles_aides.pdf

6) Funding rates
For Flanders

	Percentage of the national subsidy to the beneficiaries

Type of Organisation / Type of activity	Large Enterprises, Groups and Associations of Enterprises	Medium Enterprises	Small Enterprises	Public Research Institutes and Universities (2) (3)
Industrial/Applied Research projects	65%-JU	70%-JU	70%-JU	= JU (1:1 ratio)
Experimental development projects	40%-JU	50%-JU	60%-JU	= JU (1:1 ratio)

Notes:

1. These percentages are <u>maxima</u> and given under the constraints that the project proposal fulfils the Chips JU eligibility criteria and that no participant in the Chips JU project holds more than 70% of the total (international) Chips JU project budget.
2. The funding of stand-alone Strategic Research Centre contributions is determined by specific project related agreement with VLAIO. These projects have no specific funding limit. The eligible costs for these projects may be set equal to the Chips JU eligible costs.
3. The funding of public research institutes and universities in projects initiated by enterprises in Belgium, is determined by the general principles of O&O-bedrijfsprojecten as published on the websites
   www.vlaio.be/nl/subsidies-financiering/onderzoeksproject/wat-houdt-de-subsidie-onderzoeksproject
   www.vlaio.be/nl/subsidies-financiering/ontwikkelingsproject/wat-is-een-ontwikkelingsproject

In case of non-SOC RTO participation, the funding level of the participating (initiating) enterprise applies. The participating (initiating) enterprises are to cover the non-funded costs. Except for stand-alone Strategic Research Centre projects, funding is limited to € 3M per project. Total funding for FIO funded projects (non SOC) may be limited to € 4M. Funding to enterprises may be limited if combined R&D funding (national and Joint Undertaking) to an enterprise exceeds VLAIO applicable ruling, part of the extended eligibility criteria.

For Brussels:

Type of Organisation / Type of activity	Percentage of the national subsidy to the beneficiaries

	Large Enterprises, Groups and Associations of Enterprises	Medium Enterprises	Small Enterprises	Public Research Institutes and Universities
Industrial/Applied Research projects	65%-JU%	75%-JU%	80%-JU%	100%-JU%
Experimental development projects	40%-JU%	50%-JU%	60%-JU%	100%-JU%

Notes:
These percentages are maxima and given under the constraints that the project proposal fulfils the Chips JU eligibility criteria and that no participant in the Chips JU project holds more than 70% of the total (international) Chips JU project budget.
Project funding for Brussels may be limited to € 0,5M.

For Wallonia:

Type of Organisation / Type of activity	Percentage of the regional subsidy to the beneficiaries				
	Large Enterprises, Groups and Associations of Enterprises	Medium Enterprises	Small Enterprises	Universities	Accredited Research Centers
Industrial/Applied Research projects	65%-JU%	75%-JU%	80%-JU%	100%-JU%	75%-JU%
Experimental development projects	40%-JU%	50%-JU%	60%-JU%	100%-JU%	75%-JU%

Notes:

1. These percentages are **maxima** and given under the constraints that the project proposal fulfills the Chips JU eligibility criteria and that no participant in the Chips JU project holds more than 70% of the total (international) Chips JU project budget.

2. The proposed research activities will be qualified 'industrial research' or 'experimental development' according to the above-mentioned Walloon decree. The funding of Experimental Development projects might be carried out by means of recoverable advances (Taux de financement des projets internationaux_2021.pdf).

Additional Information to be provided at submission and other conditions

For Flanders:

Additional information is mandatory as of the FPP-phase. Application according the Chips JU application form www.vlaio.be/nl/media/739 is mandatory (endorsing the application compulsory by Chips JU FPP closing date). European application format is requested. Starting the application procedure (without endorsement) is recommended as of the Chips JU PO phase.

For Brussels

The submission of a Part C containing additional information is compulsory for all Brussels partners. The Part C template is available on the INNOVIRIS website https://innoviris.brussels/ (get-funded/ Collaboration/ECSEL).

For Wallonia:

The submission of a Part C containing additional information is compulsory for all Walloon partners. The Part C template is available on the website (www.recherche.wallonie.be).

Belgium – Innoviris Brussels

National contact person for Chips JU programme

Country	Name	First	Phone	email
BE - Brussels	Maas	Stijn	+3226005067	smaas@innoviris.brussels

(Web site or any other information source of the national funding authority as a reference to the applicants.)

INNOVIRIS: www.innoviris.brussels

1. Legal requirements for the eligibility of a partner or a project

a) Type or nature of participants

- Companies, universities or research organisations established on the territory of the Brussels-Capital Region and performing RDI activities within the project.

b) Legal, administrative and financial conditions

- A Legal organisation that develops all or part of its R&D activities in the Brussels-Capital Region.
- The company is not in difficulty, in accordance with the European legislation (p.19, point 18)
- The R&D project presents the development, completion or implementation of an innovative product, process or service.
- Prove the ability to fund the own share of the cost of the program.
- having fulfilled all obligations under previous funding granted by the Brussels-Capital Region.
- No other public funding (except the European contribution provided by the JU) can be received by the beneficiaries for the activities performed within the project. Any other funding must be declared to Innoviris.

c) Consortium configuration

- None of the partners can have more than 70% of the total project budget
- Participants in CHIPS JU projects wishing to receive funding from Innoviris must be a company or a research organisation

d) Other conditions

- Exploitation and valorisation conditions:

  Brussels-based participants must demonstrate their capability to carry out the tasks assigned to them in the project, exploit the results of the latter and the project's likelihood to have a positive impact on the Brussels-Capital Region from a social, environmental and the regional ecosystem perspective (economy, employment, sustainable development, inequalities, working conditions, well-being, …).

2. Eligibility of the costs and funding

a) Eligibility of costs

For CHIPS JU projects, the Brussels-Capital Region will align on the JU and will therefore not apply additional rules, such as the regional rules applicable for individual RDI projects, on the eligibility of costs. The eligible costs will therefore be those retained by the JU for the European contributions in accordance with the Horizon Europe Rules for Participation.

b) National public funding rates

Type of action/Type of Beneficiary	**Large enterprise**	**SME**	**Public Research Institutes and Universities**
Research and Innovation Action	65%	Small: 80% Medium: 75%	100%
Innovation Action	40%	Small: 60% Medium: 50%	100%

c) Additional Information to be provided at submission and other conditions.

The submission of a Part C containing additional information is compulsory for all Brussels partners. The Part C template is available on the INNOVIRIS website https://innoviris.brussels/

Czechia

National contact person for Chips JU programme

Country	Name	First	Phone	email
Czechia	Vávra	Michal	+420 773 793 439	Michal.Vavra@msmt.cz

(Web site or any other information source of the national funding authority as a reference to the applicants.)

Ministry of Education, Youth and Sports (https://www.msmt.cz/vyzkum-a-vyvoj-2/spolecne-technologicke-iniciativy-5-1**)**

3. Legal requirements for the eligibility of a partner or a project

e) Type or nature of participants

Public universities, public research institutes, private research organisations and/or other legal entities that can be classified as **"research and knowledge-dissemination organisations"** (hereinafter referred to as the "research organisation") in accordance with the Commission Regulation (EU) No 2021/1237 of 23 July 2021 amending Regulation (EU) No 651/2014 declaring certain categories of aid compatible with the internal market in application of Articles 107 and 108 of the Treaty (Chapter I, Article 2, Paragraph 83).

"Enterprises" – Small, medium and/or large-sized enterprises as defined by the Commission Regulation (EU) No 2021/1237 of 23 July 2021 amending Regulation (EU) No 651/2014 declaring certain categories of aid compatible with the internal market in application of Articles 107 and 108 of the Treaty (Chapter I, Article 2, Paragraphs 2 and 24), listed in Business Register of the Czech Republic and performing research, development and innovation in the Czech Republic.

f) Legal, administrative and financial conditions

Public funding of research, development and innovation in the Czech Republic is provided pursuant to the **Act No. 130/2002 Coll. on the Support of Research, Experimental Development and Innovation from Public Funds** and on the Amendment to Some Related Acts (hereinafter referred to as the "Act on the Support of Research, Experimental Development and Innovation").

g) Consortium configuration

The Czech fraction of a Chips JU project consortium in the ECS R&I calls must be configured from at least one enterprise registered in the Czech Republic and at least one research organisation, both these entities fulfilling the requirements stipulated in the clause 1 "Type or nature of participants", thus complying with the Public-Private-Partnership principle. For Chips for Europe Initiative calls, due to a different type of the calls, such a condition is not foreseen.

h) Other conditions

It is obligatory that a Czech participant involved in a Chips JU project consortium proves its compliance with the eligibility criteria and fulfilment of the conditions stipulated by § 18 of the Act on the Support of Research, Experimental Development and Innovation by the means of a **Statutory Declaration**. The required procedures are described and the Statutory Declaration template is available on the website https://www.msmt.cz/vyzkum-a-vyvoj-2/spolecne-technologicke-iniciativy-5-1.

Furthermore, applicants that seriously breached their obligations towards the MEYS, acting as the NFA, stemming from the applicable legislation or the Grant Agreement issued by the MEYS during validity of the Chips JU programme or any of its predecessors, shall be considered ineligible for the national funding.

4. Eligibility of the costs and funding

d) Eligibility of costs

Eligible costs for a Czech participant involved in a Chips JU project consortium are defined by:

Either Regulation (EU) 2021/695 of the European Parliament and of the Council of 28 April 2021 establishing Horizon Europe – the Framework Programme for Research and Innovation, laying down its rules for participation and dissemination, and repealing Regulations (EU) No 1290/2013 and (EU) No 1291/2013; Regulation (EU, Euratom) 2018/1046 of the European Parliament and of the Council of 18 July 2018 on the financial rules applicable to the general budget of the Union, amending Regulations (EU) No 1296/2013, (EU) No 1301/2013, (EU) No 1303/2013, (EU) No 1304/2013, (EU) No 1309/2013, (EU) No 1316/2013, (EU) No 223/2014, (EU) No 283/2014, and Decision No 541/2014/EU and repealing Regulation (EU, Euratom) No 966/2012. In such a case the **maximum indirect costs** are 25 % (flat rate) of the direct costs without the sub-contracting.

or Regulation (EU) 2021/694 of the European parliament and of the Council of 29 April 2021 establishing the Digital Europe Programme and repealing Decision (EU) 2015/2240. In such a case the **maximum indirect costs** are 7 % (flat rate) of the direct costs without the sub-contracting.

The legislative framework defined for the eligibility of costs reflects the EU funding

programme from which the EU support is provided and the rules of eligibility that are applied by the European Commission (either Horizon Europe, or Digital Europe).

e) National public funding rates

The MEYS consider the Research and Innovation Actions (RIA) being industrial research projects and the Innovation Actions (IA) being experimental development projects. Given these circumstances, the maximum intensity of the MEYS aid will be derived from the Commission Regulation (EU) No 2021/1237 of 23 July 2021 amending Regulation (EU) No 651/2014 declaring certain categories of aid compatible with the internal market in application of Articles 107 and 108 of the Treaty (Chapter III, Section 4, Article 25, Paragraph 5).

The maximum aid intensity for industrial research and experimental development will not be increased by the MEYS although the Czech participants in a Chips JU project consortium meet the conditions stipulated by the Commission Regulation (EU) 2021/1237 of 23 July 2021 amending Regulation (EU) No 651/2014 of 17 June 2014 declaring certain categories of aid compatible with the internal market in application of Articles 107 and 108 of the Treaty (Chapter III, Section 4, Article 25, Paragraph 6). The maximum aid intensities stipulated in the table below are definitive.

Type of action/Type of Beneficiary	**Large enterprise**	**Small and medium sized enterprises**	**Research organisations***
Research and Innovation Actions (RIA) projects = **Industrial Research**	50 % including EU contribution	70 % including EU contribution	100 % including EU contribution
Innovation Actions (IA) projects = **Experimental Development**	40 % including EU contribution	50 % including EU contribution	100 % including EU contribution

* **The aid intensity for research and development activities carried out by the research organisation might be at the level of 100 % (EU and the Czech national contribution included)** only if the research organisation entirely complies with the requirements stipulated by the Article 2.1.1 "Public funding of non-economic activities" of State aid framework for research and development and innovation (2022/C 414/01) and proves it by the means of a **Statutory Declaration** submitted to the MEYS using the form available on website https://www.msmt.cz/vyzkum-a-vyvoj-2/spolecne-technologicke-iniciativy-5-1.

If a legal entity does not comply with all the requirements stipulated for the research organisation, it will be considered as an enterprise (small, medium or large) and the aid intensity will be then adjusted appropriately by the MEYS.

f) Additional Information to be provided at submission and other conditions.

All the information concerning additional requirements stipulated by the MEYS for the Chips JU programme are available on website https://www.msmt.cz/vyzkum-a-vyvoj-2/spolecne-technologicke-iniciativy-5-1.

Cyprus

Total Budget for WP 2024 (ECS): € 2.000.000
Max. Funding Per Project: € 500.000
Funding Agency: Research and Innovation Foundation (RIF)

National Contact Points for KDT/Chips JU Programme

Country	Surname	Name	Email	Tel.
CYRPUS	Portokallides	Marinos	mportokallides@research.org.cy	+35722205052

A. Specific Restrictions and Conditions for Participation

All general rules and procedures for the participation of organisations and individuals, the eligible activities and costs, as well as the specific information regarding the «Innovation Vouchers» Programme, as well as the other RESTART 2016-2020 Programmes, are included in the RIF's Work Programme for the «RESTART 2016-2020» Programmes for Research, Technological Development and Innovation, which is the main reference document and an important information source for interested parties.

Furthermore, specific information for each Call can be found in the relevant National Call Documents:

- **EP/KDT-CHIPS-IA/0324**
- **EP/KDT-CHIPS-IA-FT/0324**
- **EP/KDT-CHIPS-RIA/0324**

1) Beneficiaries

Host Organisation (of the Cypriot Consortium) could be an Enterprise, a Research Organisation or an Other Private or Public Organisation.

Research Organisations, Enterprises and Other Private or Public Organisations can participate as Partner Organisations (in the Cypriot Consortium).

Maximum number of organisations in the Cypriot Consortium should be between one to three (1-3).

Participation of Large Enterprises is only permitted when an SME is also participating in the Cypriot Consortium.

Participation of startups is not allowed except for those with marketable products/services, with a record for sales and turnover and audited financial statements for at least two (2) years.

Each Enterprise can receive funding from the RIF for a maximum of two (2) Projects in the frame of «European Partnerships – Key Digital Technologies» Programme during the 2021-2027 period.

For Innovation Actions:

- The participation of an SME in the Cypriot Consortium is obligatory.
- At least 30% of the Cypriot consortium's participants budget should be allocated to Enterprises.

2) National Application

The Coordinator of the Cypriot Consortium should also submit a Proposal on the RIF's IRIS Portal (https://iris.research.org.cy). The Project Coordinator and all local participating organizations of the Cypriot Consortium, should register in advance on the IRIS Portal.

Potential applicants are advised to read the **«Guide for Applicants»**, which contains guidelines and clarifications regarding the Submission procedure and the **«IRIS Portal User Manual»** which can be found on the IRIS Portal (https://iris.research.org.cy/#/documentlibrary).

The Proposal submitted to the RIF includes only general information regarding the Transnational Proposal (Title, Acronym etc), the Coordinator of the Cypriot Consortium and the partner organisations of the Transnational Consortium (including the Cypriot organisations) as well as detailed budget for each partner participating in the Cypriot Consortium. The budget of each organization should be the same with the budget to be included in the Proposal submitted to the EU.

The Project Proposal consists of the following parts:

1. Part A – General Information & Budget (electronic form (fields) to be completed online through the IRIS Portal).
2. ANNEX II – Call Specific Information to be disclosed to the Evaluators – **Mandatory Submission** (document to be uploaded as an Annex on the IRIS Portal in PDF format and includes the «SMART SPECIALISATION SECTORS (S3Cy 2023-2030)» Table for the selection of the Priority Sector/ of the Smart Specialisation Strategy that the Proposal is applied to). *The relevant document is available in IRIS Portal, under the specific Call (Call Documents). The selection is obligatory and should be limited to only one Priority Sector.*
3. ANNEX III – Call Specific Information – **Mandatory Submission** (document to be uploaded as Annex on the IRIS Portal in PDF format): *Financial Statements: Audited Financial Statements of the Host Organisation for the previous financial year or the year preceding it, for the purposes of preliminary and financial viability check – Obligatory Submission. Organisations undergone a financial viability check by the RIF in the frame of previous contract preparation, with valid financial viability check results, are exempted.*

Eligibility of Costs and Funding

National Calls will be co-financed by the Republic of Cyprus and the European Regional Development Fund (ERDF), in the frame of the Operational Programme «ΘΑλΕΙΑ» 2021-2027 under Priority 1: «Competitive, Smart and Digital Economy» and the Specific Objective (1i): «Developing and enhancing research and innovation capacities and the uptake of advanced technologies».

1) Eligible Costs

Personnel costs, Instruments and Equipment Costs, Costs for External Services, Costs for Travelling Abroad, Consumables, Other Specific Costs, Overheads.

It is noted that, all beneficiaries that have not previously participated in the RESTART 2026-2020 Programmes, should make use of the simplified cost Method «Standard Scales of Unit Costs» for the calculation of personnel costs.

Eligible Costs are described in the RIF's Work Programme for the «RESTART 2016-2020» Programmes for Research, Technological Development and Innovation.

2) Funding Rates

	Small Enterprise	**Medium Enterprise**	**Large Enterprise**	**«Research Organisations» and «Other Public and Broader Public Sector Organisations»**
HORIZON-Chips 2024-1-IA T1 ***(Experimental Development Activities)***	30%	20%	20%	65%
HORIZON- Chips 2024-1-IA T2 **HORIZON- Chips 2024-1-IA T3** ***(Experimental Development Activities)***	30%	20%	15%	65%
HORIZON- Chips 2024-2-RIA T1 **HORIZON- Chips 2024-2-RIA T2** ***(Industrial Research Activities)***	45%	40%	40%	65%

Denmark – Innovation Fund Denmark (IFD)

National contact persons for Chips JU program

For specific questions regarding eligibility to national co-funding or the national application procedure, please contact **Innovation Fund Denmark (IFD)**:

Country	Last Name	First name	Telephone	E-mail
Denmark	G. Marques	Daniel	+45 6190 5006	daniel.g.marques@innofond.dk
	Holm Tveen	Mathias	+45 6190 5073	mathias.holm.tveen@innofond.dk
	General contact		N/A	internationale@innofond.dk

For specific questions regarding Danish interested groups and international consortia, please contact the **Danish Agency for Higher Education and Science (UFS)**:

Country	Last Name	First name	Telephone	E-mail
Denmark	Lange	Alexandra	+45 7231 7937	alel@ufm.dk
	Humer	Matthias	+45 7231 8710	matu@ufm.dk

Unless otherwise specified in this Annex, the IFD's Guidelines for International Projects apply. Please find **IFD's Guidelines for International Projects**, templates for required documentation, and additional supporting information here (full link below):

- https://innovationsfonden.dk/en/p/international-collaborations

Legal requirements for the eligibility of a partner or a project for calls in the Work Programme 2025

1. Type or nature of participants

- All Danish organizations directly involved in activities in the projects are eligible as applicants to IFD.

2. Legal, administrative and financial conditions

- Please refer to IFD's Guidelines for International Projects (link at the top).

3. Consortium configuration

- No national requirements regarding consortium configuration, unless specified under conditions for maximum national funding. Innovation Fund Denmark encourages Danish applicants to maximize impact in Denmark, as well as cross-sectoral collaborations.

4. Other conditions

- Danish applicants must access the national e-grant system and provide the requested documentation.
- Usually 2-4 weeks after the central submission deadline, Danish applicants will receive a request to access their case in the national e-grant system. Applicants will be requested to:
    - Upload the international project proposal, including annexes and budgets.
    - Further mandatory documentation will be requested to non-public organisations via e-grant. The templates for the mandatory documentation can be found under Documents (link also at the top).
- In case the application is selected for funding, Danish applicants are required to submit a consortium agreement signed by all project participants before the start of the project, according to IFD's Guidelines.

Eligibility of the costs and funding for calls in the Work Programme 2025

1. Eligibility of costs

The eligibility of costs is regulated by the IFD's Guidelines for International Projects. Eligible costs:

- Salaries
- Travel
- Subcontracting
- Materials
- Communication and knowledge sharing
- Other expenses
- Overhead (according to the applicable rates, see below).

2. National funding

Both maximum and minimum funding *amounts* and maximum funding *rates* apply.

Maximum national funding amounts

Maximum national funding of **650.000 EUR** per project (if there is more than one Danish partner) and maximum **650.000 EUR** per Danish partner. If the coordinator is a Danish organisation, then the maximum national funding is **1.300.000 EUR** per project and **650.000 EUR** per Danish partner. These are higher maximum funding amounts than the standard indicated in the Guidelines for International Projects. The minimum funding amount is **50.000 EUR** per partner. EU co-funding is not included in the maximum and minimum national funding amounts.

Maximum national funding rates

The maximum national funding rates are regulated by the Guidelines for International projects. Maximum national funding rates depend on the applicant's type of organisation. In addition, applicants may be eligible for EU co-funding according to the Chips JU criteria and maximum co-funding rates.

Maximum national funding rates are given in the table below in relation to the national eligible costs.

Maximum national funding rates[26]					
Call		**Large Enterprises***	**SMEs***	**GTS and other Research Institutes**	**Universities and other public entities**
ECS	Global RIA Call (Industrial Research)	40 %	40 %	25 %	55 %
	Global IA Call (Experimental Development)	20 %	20 %		
	IA Focus Topics Calls FT1 and FT2 (Experimental Development)	15 %	15 %		
	Heterogeneous integration for high-performance automotive computing Call (Experimental Development)				

[26] Contact IFD before application for information on the maximum national funding rates for approved Danish national cluster organisations and requirements for organisations with the special status of research and knowledge dissemination institutions, as defined in IFD's Guidelines (link at the top).

Chips for Europe Initiative	Low power Edge AI Chips Call (Experimental Development)				
	Accelerator for Advanced sSOI (Experimental Development)				
	Lab to Fab Accelerator (Experimental Development)				
	Open-source EDA tools development Call (Experimental Development)	20 %	20 %	10 %	40 %

*All organisations carrying out economic activities in the project are considered as enterprises.

National maximum funding rates are adjusted to Chips JU maximum EU co-funding rates so that the total maximum funding rates (national and EU co-funding) follow IFD's standard maximum funding rates according to the Guidelines for International Projects[27].

Special funding rules for the calls for Quantum Pilots (SGA-QAC1 and SGA-QAC2)

For these specific calls, the funding is regulated by the **Annex to the Guidelines for International projects** published at IFD's call announcement.

The **maximum national funding rate is 50% for all types of organisations**. No maximum national funding amounts apply per partner or per project besides the available budget for the calls. In addition, applicants may be eligible for EU co-funding according to the Chips JU criteria and maximum co-funding rates.

Rates for indirect costs (overhead)

Applicable overhead rates according to the Guidelines for International Projects. Costs with subcontracting are not eligible for overhead.

[27] National funding will be subject to conditions in current state aid rules (Commission Regulation (EU) No 651/2014). If other public funding, besides the EU funding, will be granted for the project, the listed maximum rates for national funding will be reduced if required to ensure that aid intensity limits in the state aid rules are respected. Beneficiaries must submit declarations regarding company size and financial situation.

Rates for indirect costs (overhead)[1]			
Universities and public research institutions	**Approved Danish National Cluster Organisations**	**Danish GTS**	**Others**[28]
44 %	20 %	0% (salaries are multiplied by the GTS cost factor)	0 %

[28] For Public Hospitals the overhead rate is 3,1 %.

Estonia

National contact person for Chips JU programme

Country	Name	First	Phone	email
Estonia	Vedina	Rebekka	+372 56976673	rebekka.vedina@etag.ee
	Suuroja	Margit	+372 731 7360	margit.suuroja@etag.ee

Estonian Research Council www.etag.ee

The full version of the national eligibility criteria can be found at: Lisa_Vastavusnõuded RV ühiskonkurssidel (etag.ee)

1. Legal requirements for the eligibility of a partner or a project

a) Type or nature of participants

The Host Institution could be any legal entity that is registered and located in Estonia and has an Estonian bank account.

The Host Institution (the final recipient) is the institution to which the grant will be allocated.

The Principal Investigator is a researcher who acts as the Estonian team leader in the project proposal. The Principal Investigator will be responsible for how the grant is used and how the Estonian part in the project is executed.

b) Legal, administrative and financial conditions

The Host Institution:

After the submission deadline (in case of two-stage application, after the preproposal deadline) and upon the notice from the Estonian Research Council, the Host Institution must confirm to the Council in the written form that the project can be carried out on their premises in Estonia and that they will employ the Principal Investigator during the proposed project, should the project receive funding.

If the Host Institution is a for-profit institution, the State aid and de minimis aid regulations must be taken into account. For details on State aid and de minimis aid please see the full version of the national eligibility criteria at Lisa_Vastavusnõuded RV ühiskonkurssidel (etag.ee)

If the State aid or de minimis aid regulations apply, the funding will not be granted to a Host Institution who has been subject to a funding withdrawal decision pursuant to a previous European Commission decision that deemed the aid illegal and incompatible with the common market, if that decision has not been complied with.

In case of a positive financing decision the Host Institution and the Estonian Research Council will enter into a bilateral agreement. Information on the transnational project must be entered into ETIS once the agreement has been signed.

The Principal Investigator:

- must have an updated public profile in the Estonian Research Information System (ETIS) by the submission deadline;

- must hold a doctoral degree or an equivalent qualification. The degree must be awarded by the submission deadline of the grant application;

- must have published at least three articles that comply with the requirements of Clause 1.1 of the ETIS classification of publications, or at least five articles that comply with the requirements of Clauses 1.1, 1.2, 2.1 or 3.1, within the last five calendar years prior to the proposal submission deadline. International patents are equalled with publications specified under Clause 1.1. A monograph (ETIS Clause 2.1) is equalled with three publications specified in Clause 1.1 if the number of authors is three or fewer.

If the Principal Investigator has received the PhD degree outside Estonia, its correspondence to an Estonian doctoral degree must be recognised by either the Estonian ENIC-NARIC Center or the Host Institution in accordance with the Regulation of the Government of the Republic of April 6, 2006, No. 89 "Evaluation and academic recognition of documents proving foreign education and the name of the qualification awarded in the foreign education system terms and conditions of use". The Estonian Research Council may ask for a relevant Evaluation Report[29].

If several Estonian institutions participate in a proposal, all institutions must have a Principal Investigator who meets the national eligibility criteria.

c) Consortium configuration

Each partner in a funded project will be funded by their national Funding Organisation. It is mandatory for all Estonian applicants to follow the national eligibility criteria. Please note that if one of the partners is not eligible, the entire proposal might be considered ineligible.

The Consortium Agreement should be signed at the latest six months after the grant agreement has been signed. If one year has elapsed and the CA has not been signed, the next instalment of funding will not be paid out.

d) Other conditions

If human research or animal testing are intended in the project, a positive resolution by the Human Research Ethics Committee or the Authorisation Committee for Animal Experiments must be submitted to the Estonian Research Council by the start of the relevant activities.

By applying for funding by the Estonian Research Council, the applicants agree to consider the relevance of the Nagoya protocol for their research, and to submit the Due Diligence Declaration, if applicable.

Following the restrictions laid down in Article 7 of the Regulation of the European Parliament and of the Council No 2021/1058 of 24 June 2021 on the European Regional Development Fund and on the Cohesion Fund[30] research and other activities related to fossil

[29] The required documents and procedure, including the application form can be found on the web page https://www.harno.ee/en/enicnaric. The evaluation period can take up to 30 days.
[30] https://eur-lex.europa.eu/legal-content/EN/TXT/PDF/?uri=CELEX:32021R1058

fuels and their use, as well as other activities not eligible as per Article 7 of the Regulation, cannot be funded from the European Regional Development Fund (Mobilitas 3.0) resources.

2. Eligibility of the costs and funding

i. Eligibility of costs

Research expenses consist of direct costs (personnel costs, travel costs and other direct costs) and subcontracting costs. The research expenses must be used to carry out the project and be separately identifiable.

Direct costs

1. Personnel costs are monthly salaries with social security charges and all the other statutory costs of the project participants, calculated according to their commitment and in proportion to their total workload at their Host Institution.

2. Travel costs may cover expenses for transport, accommodation, daily allowances and travel insurance only for travels abroad.

3. Other direct costs are:

- consumables and minor equipment related to the project;
- publication and dissemination of project results;
- organising meetings, seminars or conferences (room rent, catering);
- fees for participating in scientific forums, conferences and other events related to the project;
- patent costs;
- all other costs that are identifiable as clearly required for carrying out the project (e.g. translation, copy editing, webpage hosting, etc.) and comply with the eligible costs.

Subcontracting costs should cover only the additional or complementary research related tasks (e.g. analyses, conducting surveys, building a prototype, etc.) performed by third parties. Subcontracting costs should not be included in the overhead calculation. The activities and budget should be described in the proposal. Core project tasks should not be subcontracted. Subcontracting costs may not exceed 15% of the total costs.

Indirect costs (overhead) may not exceed **15% of the personnel costs** and should cover the general expenses of the Host Institution. Costs for equipment and services intended for public use (a copy machine or a printer that is publicly used, phone bills, copy service, etc.) should be covered from the overhead.

Double funding of activities is not acceptable.

If several Estonian institutions participate in one proposal, the sum of their requested budgets may not exceed the maximum contribution of the respective national Funding Organisation indicated in the call documents.

ii. National public funding rates

Type of action/Type of Beneficiary	**Large enterprise**	**SME**	**Public Research Institutes and Universities**
Research and Innovation action	yes	yes	yes

Innovation Action	yes	Yes	yes

Estonian Research Council funds a successful participant with up to 300 000 EUR for consortium coordinator or up to 150 000 EUR for consortium partner. The total funding for ECS calls 2024 is 300 000 EUR.

Finland

National contact person for Chips JU programme

Country	Name	First	Phone	email
Finland	Ahola	Kimmo	+358 50 5577 756	kimmo.ahola@businessfinland.fi
	Ihanus	Veli-Pekka	+358 40 7046 362	veli-pekka.ihanus@businessfinland.fi

Finland's national public funding authority is *Innovation Funding Agency Business Finland*.
The evaluation of each participant's eligibility for funding is carried out using the criteria for Business Finland national R&D funding.

Business Finland funding principles can be found at:
www.businessfinland.fi/en (English)
www.businessfinland.fi (Finnish)

1. **Legal requirements for the eligibility of a partner or a project**

a) Type or nature of participants

- Companies (enterprises)
- Industry associations
- Universities and polytechnics
- Public research institutes and similar research organizations.

b) Legal, administrative and financial conditions

- A company has considerable industrial or R&D&I activities in Finland.
- A company has a clear financial record and has the financial capability to cover its own expenses during the project
- Funding cannot be granted to a company that is a 'firm in difficulty' according to the EU definition.

c) Consortium configuration

- Research and Innovation Actions (RIA) projects: A public research institute, university or a polytechnic shall be accompanied in the project by at least three companies (Partner or Associated) in Finland. The project volume (costs) of public

research institutes, universities and polytechnics from Finland combined shall not exceed 70 % of the total volume (costs) of Finnish participants based on national Business Finland funding rules.

- Innovation Action (IA) projects: A public research institute, university or a polytechnic shall be accompanied in the project by at least two eligible (Partner) companies in Finland. The project volume (costs) of public research institutes, universities and polytechnics from Finland combined shall not exceed 30 % of the total volume (costs) of Finnish participants based on national (Business Finland) funding rules.

d) Other conditions

- The project participation must aim for significant business and export growth as well as have sufficient positive impact on the Finnish economy or society.
- Priority is given to topics that are not covered by already funded projects.
- Priority is given to projects that facilitate and implement strong international cooperation between companies.

2. Eligibility of the costs and funding

a) Eligibility of costs

- Eligibility of the costs is in accordance with the national (Business Finland) funding rules.

b) National public funding rates

Type of action/Type of Beneficiary	**Large enterprise**	**SME**	**Public Research Institutes and Universities**
Research and Innovation action	20 % grant	35 % grant	38 % grant
Innovation Action	20 % grant	35 % grant	38 % grant

c) Additional Information to be provided at submission and other conditions.

Every participant from Finland must submit a separate Business Finland funding application within 14 days of the call Full Proposal closure date.

France

National contact person for Chips JU programme

Country	Name	First name	Tel	E-mail
France	RITOU	Arnaud	+33 1 53 18 36 16	arnaud.ritou@finances.gouv.fr
	BEDOUET	Loane	+33 1 53 18 20 97	loane.bedouet@finances.gouv.fr

Website reference: https://www.entreprises.gouv.fr/fr/numerique/enjeux/soutien-la-nanoelectronique

Exigences légales pour l'éligibilité d'un partenaire ou d'un projet.

The items published in French in the following text are the official national eligibility criteria for funding. The following items published in English are a translation. The text in French takes precedence over the text in English.

Les porteurs français d'une proposition de projet pour un appel à projets Chips JU en 2025 doivent, pour être éligibles, avoir été retenus pour ce projet par un mécanisme de financement national:

- au titre du **volet français** du PIEEC électronique et connectivité, s'ils en sont bénéficiaires et dans les conditions prévues par le programme ;
- au titre d'un appel à projets national ou régional, en respectant les conditions spécifiques à cet appel.

Les partenaires doivent impérativement contacter les correspondants nationaux indiqués au début de cette annexe avant le dépôt de la « Project Outline » (pour les appels en deux phases) ou de la proposition finale (pour les appels en une seule phase).

L'objectif de ce contact est d'orienter le demandeur vers le guichet le plus adapté, de préparer l'examen des critères d'éligibilité nationaux, et pour les chefs de file du PIEEC électronique et connectivité, de préciser les démarches à mener afin de déterminer la conformité du projet avec les axes stratégiques du programme.

Financement dans le cadre du volet français du PIEEC électronique et connectivité

Les critères suivants ne s'appliquent qu'aux porteurs de projets retenus au titre du programme national (sans nom à date) dans le cadre du **volet français du** PIEEC électronique et connectivité et ne préjugent

pas de l'application des règles légales et règlementaires en vigueur concernant l'attribution de subventions par l'État français.

Pour les partenaires ayant déposé une demande de financement au titre d'un appel à projets national ou régional, ils doivent se référer au cahier des charges de l'appel à projets en question.

1) Type ou nature des participants

- Entreprises privées ou publiques de toutes tailles
- Universités
- Instituts de recherche

2) Conditions légales, administratives et financières

Les travaux ne doivent pas déjà avoir fait l'objet d'un soutien public (hors mesures fiscales génériques) ni être en redondance avec des travaux similaires financés par les autorités françaises, ni avoir été engagés avant la date de début du projet indiqué dans la « Full Project Proposal »

La situation financière de chaque partenaire privé doit être validée (structure financière, flux de trésorerie, compte d'exploitation) et jugée compatible (volume d'activité, moyens humains, moyens financiers) avec le montant et le contenu de l'assiette des dépenses ainsi qu'avec le montant de l'aide sollicitée et des aides publiques déjà accordées par ailleurs.

3) Cohérence avec le PIEEC électronique et connectivité et le plan France 2030

Les porteurs de projets doivent s'intégrer dans les objectifs globaux du PIEEC électronique et connectivité, et contribuer à lever un ou plusieurs verrous technologiques significatifs en vue de concevoir ou d'améliorer des produits, services ou procédés, ainsi que mettre en place les moyens de réalisation de ces produits et procédés. Ceux-ci doivent présenter pour eux des perspectives suffisantes de retombées sur le territoire de l'Union européenne, et notamment en France, en termes d'emplois, de compétitivité, de création de valeur et d'activité économique à court ou moyen terme.

Les propositions doivent comporter la participation d'au moins un chef de file français du PIIEC électronique et connectivité. Néanmoins, la coordination et le dépôt de la proposition peuvent être confiés à un autre partenaire du consortium.

Les travaux réalisés par les porteurs doivent être bien spécifiés et pouvoir être considérés comme « développement expérimental » ou « recherche industrielle » au sens de l'encadrement des aides d'Etat à la RDI. Conformément à ce régime d'aide, l'aide à chaque entreprise doit avoir un effet d'incitation sur ses activités de RDI.

Les partenaires doivent remplir les conditions d'éligibilité propres aux partenaires du PIEEC électronique et connectivité :

- déposer un dossier complet, au format imposé, sous forme électronique via la plateforme de Bpifrance,
- dont les modalités d'accès seront précisés par le contact national indiqué en début de cette

annexe ;

Intégrant les priorités de France 2030, l'aspect « émergent » ou « en développement » est un point particulier de sélection des partenaires de projets dans la mesure où France 2030 vise à faire émerger de nouveaux acteurs économiques.

Ainsi, les projets intégrant des acteurs tels que des entreprises de moins de 12 ans ou des PME/ETI opérant un pivot stratégique radical, les amenant à développer de nouveaux produits très innovants en rupture ou qui concernent des marchés émergents, ou en très forte croissance, ou procédant à des opérations de build-up avec des entreprises de moins de 3 ans ou encore en consortium de R&D collaborative avec des start-ups seront privilégiés.

4) Coûts éligibles

Les coûts éligibles français seront basés sur le montant obtenu en remplissant les annexes financières disponible sur la plateforme de Bpifrance, pour chaque partenaire français.

5) Taux de soutien

Type d'entreprise / Type de recherche	Grande entreprise (GE et ETI)	PME	Organisme de recherche en coûts marginaux	Organisme de recherche en coûts complets
Research and Innovative Action (RIA) **&** **Innovative Action (IA)**	20 %	30 %	100 % moins aide demandée à la JU	35%

6) Informations nécessaires à la soumission

Pour les porteurs éligibles au programme national (sans nom à date) dans le cadre du volet français PIEEC électronique et connectivité, et en complément du dossier de soumission du projet, transmis à l'entreprise commune, le responsable français de chaque projet doit adresser aux autorités françaises, un dossier sur la plateforme de Bpifrance consacrée dont le contact national lui précisera les modalités d'accès.

Le dossier soumis doit présenter les éléments permettant aux autorités françaises d'apprécier et de justifier l'admissibilité de l'aide demandée par le porteur et ses partenaires. En particulier, le dossier doit comprendre, outre les documents requis au titre de l'appel à projets de l'entreprise commune, les documents spécifiés sur la plateforme mentionnée précédemment.

Financement dans le cadre d'appels à projets nationaux ou régionaux

Les partenaires ayant déposé une demande de financement au titre d'un appel à projets national ou régional, doivent se référer au cahier des charges des dispositifs en question pour connaitre leurs critères d'éligibilité et conditions de financements.

Des documents supplémentaires pourront être demandés, dans les conditions desdits appels à projets afin de permettre aux autorités décidant de l'octroi de l'aide, d'apprécier et de justifier l'admissibilité de l'aide demandée par le porteur et ses partenaires.

Les taux d'aide dépendront des conditions propres aux dispositifs dont les financements seront issus, et à la prise en compte par ces dispositifs de l'existence d'un cofinancement européen.

1) *Précisions relatives aux dispositifs s'inscrivant dans le cadre de France 2030*

Suivant les priorités du plan France 2030, l'aspect « émergent » ou « en développement » est un point particulier de sélection des partenaires, dans la mesure où France 2030 vise à faire émerger de nouveaux acteurs économiques.

Ainsi, les projets intégrant des acteurs tels que des entreprises de moins de 12 ans ou des PME/ETI opérant un pivot stratégique radical, les amenant à développer de nouveaux produits très innovants en rupture ou qui concernent des marchés émergents, ou en très forte croissance, ou procédant à des opérations de build-up avec des entreprises de moins de 3 ans ou encore en consortium de R&D collaborative avec des start-ups seront privilégiés.

Est notamment concerné, l'appel à projet I-Démo Europe.

À titre d'information, pour les projets dont le financement national serait obtenu au titre de l'appel à projets « I-Démo Europe », les taux prévus sont les suivants :

Type d'entreprise / Type de recherche	**Grande entreprise** (GE et ETI)	**PME**	**Organisme de recherche** (coûts complets)	**Organisme de recherche** (coûts marginaux)
Research and Innovative Action (RIA)	25 %	35 %	25%	65%
Innovative Action (IA)	20 %	30 %		

Legal requirements for the eligibility of a partner or a project
The items published in French in the following text are the official national eligibility criteria for funding. The items published in English are a translation. The text in French takes precedence over the text in English.

The indicative commitment previously indicated in this work programme, in the subpart *National Budgets for the call 2024*, is not a budget to allocate to French applicants to Chips JU calls, but an estimation of the ability of French partners to obtain national funding through mechanisms described below.

Consequently, **the French applicants of a Chips JU 2024 project proposal must, to be eligible, have been selected for this project to a national funding schemes:**

- through national program such as the French framework (successor of Nano 2022, not yet named) in the context of the upcoming IPCEI Microelectronics and Communication Technologies, if they are beneficiaries of it, and under the conditions of the program:.
- through a national or regional call, with respect to the specific conditions of this call.

Partners must contact the national correspondents before the Project Outline submission (for 2-stage calls) or before the final proposal submission (for single stage calls).

The aim of this contact is to direct the requestor to the most relevant financing mechanism, to prepare the national eligibility criteria examination, and for the French direct partner of the IPCEI ME-CT, to precise procedures to check the conformity of the project with the strategic lines of the program.

I. Funding through the French framework of the upcoming IPCEI Microelectronics and Communication Technologies

The following criteria are valid only for the applicants selected trough the French framework (not yet named) in the context of the upcoming IPCEI Microelectronic and Communication Technologies and are without prejudice to the application of legal rules and regulations concerning the allocation of public funding by the French State.

For partners who have submitted an application for funding under a national or regional call for projects, they must refer to the terms of reference of this call.

1) Type or nature of participants

- Private and public companies of all sizes
- Universities
- Research Institutes

2) Legal, administrative and financial conditions

The work to be done by the partners must neither have already benefited from public funding (excluding generic fiscal aid) nor be redundant with similar projects already funded by French authorities, nor engaged before the start date of the project indicated in the Full Project Proposal.

The financial situation of each private partner must be validated (financial structure, cash flow, operating accounts) and considered compatible (activity volume, workforce, financial capability) with the amount and the content of the eligible costs as well as with the amount of the demanded aid and of the already granted public aid.

3) Coherence with the IPCEI Microelectronics and Communication Technologies and the French investment plan FRANCE 2030

The applicants must contribute to the global objectives of the IPCEI Microelectronics and Communication Technologies and achieve one or several significant technological breakthroughs with the objective of designing or improving products, services or processes, and must set-up a capability to make these products or processes. These ones must have a sufficient potential impact on their activity in the European Union and in particular in France, in terms of employment, competitiveness, value creation and growth at short or medium-term.

The proposals shall include the participation of at least one direct partner of the IPCEI Microelectronics/Connectivity. Nevertheless, the coordination and the submission of the national proposal can be entrusted to another partner of the consortium.

The tasks assigned to applicants must be well specified and should consist in « experimental development » or « industrial research » as defined in the R&D&I framework. In accordance with the R&D&I framework, the aid to each company must have an incentive effect on its R&D&I activities.

Partners of the project have to fulfil the proper eligibility criteria of French partners of the IPCEI Microelectronics and Communication Technologies:

- Submit a complete file, in the required format, in electronic form via the Bpifrance platform. The terms of access to this platform will be provided by the national contact indicated in the beginning of this annex;

Following France 2030 support plan's priorities, the "emerging" or "developing" aspect of the project's partners is a key point of selectivity of the projects, France 2030 aiming at fostering new/emerging economic actors.

Project integrating companies less than 12 years old or project integrating companies operating a significant market or strategic reorientation towards new particularly innovative products or towards emerging markets, or experiencing an intense growth, or conducting external growth acquiring companies not older than 3 years on the relevant market or in a research and development consortium with start-ups, will be prioritized.

4) Eligibility of costs

The French eligible costs will be based on the amount obtained using the financial data sheets that can be found on the Bpifrance online platform, for each French partner.

5) Funding rates

Type of beneficiary / Type de project	Large enterprises	SMEs	RTOs (Incremental costs)
Research and Innovative Action (RIA) & Innovative Action (IA)	20 %	30 %	100 % minus aid requested to the JU

6) Additional information to be provided at submission

Applicants eligible to the French framework (not named yet) in the context of the upcoming IPCEI Microelectronic and Communication Technologies and in parallel to the documents sent to the Chips JU, the French leader of each submitted project will have to send to the French public authorities a set of documents through the dedicated platform of Bpifrance. The French national contact will precise the terms of access of this platform to the French leader of the project.

The application submitted must **contain all elements which will allow French authorities to assess and justify the eligibility of the aid** asked by the applicants. In particular, the application must include, besides the documents required for application to the Joint Undertaking call, all documents listed on the dedicated platform of Bpifrance previously mentioned.

II. Funding through national or regional calls

Partners who have submitted an application for funding under a national or regional call for projects must refer to the terms of reference of this call to know their eligibility criteria and conditions for funding.

Additional documents may be asked, as per the conditions of the relevant program, in order to allow decisional bodies to assess and justify the eligibility of the aid asked by the applicants.

Rates for funding will depend on the conditions of these calls, who could also take into account the existence of a European co-funding.

1) Details regarding calls set up under the French investment plan France 2030

According to the priorities of the French investment plan France 2030, the “emerging” or “developing” aspect of the project’s partners is a key point of selectivity of the, France 2030 aiming at fostering new/emerging economic actors.

Project integrating companies less than 12 years old or project integrating companies operating a significant market or strategic reorientation towards new particularly innovative products or towards emerging markets, or experiencing an intense growth, or conducting external growth

acquiring companies not older than 3 years on the relevant market or in a research and development consortium with start-ups, will be prioritized.

The I-Démo Europe call is particularly concerned.

For information, for projects whose national public funding originate from "I-Demo Europe" scheme, the support rates are as follows:

Type of beneficiary / **Type of project**	**Large enterprises**	**SMEs**	**RTO** (Full costs)	**RTO** (Incremental costs)
Research and Innovative Action (RIA)	25 %	35 %	25%	65%
Innovative Action (IA)	20 %	30 %		

Germany

National contact persons

Country	Name	First	Phone	email
Germany	**General information on funding under Horizon Europe**			
	Hauke	Alrun	+49 228 3821-2505	alrun.hauke@dlr.de ; nks-dit@dlr.de
	Specific information on national funding applications for the Chips JU			
	Schwartz	Gregor	+49 351 48679747	Gregor.Schwartz@vdivdeit.de
	Müller	Mathias	+49 30 310078 5471	Mathias.Mueller@vdivdeit.de
	Specific information on calls related to quantum technologies			
	Klein	Claudius	+49 221 6214 903	klein_c@vdi.de
	Hiltscher	Bastian	+49 221 6214 441	hiltscher@vdi.de

Applicable documents and further information are available via the website
www.elektronikforschung.de/foerderung/bekanntmachungen/chipsju

For calls related to quantum technologies specific information is available via
www.quantentechnologien.de

Federal funding will be awarded by the Bundesministerium für Bildung und Forschung (BMBF). Partners from Thuringia and Saxony may receive combined funding from the BMBF and the respective Land.

1. **Criteria and rules for the eligibility of a partner or a project**

a) Applicable documents

- The German Federal Government's **Framework programme** for Research and Innovation 20212024 „Mikroelektronik. Vertrauenswürdig und nachhaltig. Für Deutschland und Europa." and the funding programme "Quantensysteme"of Bundesmininisterium für Bildung und Forschung.
- The **national call** "Richtlinie zur Förderung der Mikroelektronik-Forschung von Verbundpartnern im Rahmen des Gemeinsamen Unternehmens Chips" covering research topics in electronics
- The **national call** "Richtlinie zur Förderung der Forschung zu Quantentechnologien im Rahmen des Gemeinsamen Unternehmens Chips" covering research topics in quantum technologies

b) Type or nature of participants

- Commercial companies in Germany.
- State and non-state institutions of higher education and non-university research establishments.

2. Legal requirements for the eligibility of a partner or a project

A German partner's contribution is eligible for national funding by the BMBF if it focuses on research in electronics including interdisciplinary topics (e.g. cyber-physical systems, integrated photonics, electronics for quantum technology, embedded software) or in quantum technologies as specified in the **national calls** (see above).

- If the funding requests for BMBF exceed the available funding, projects with greater contributions to the strategic objectives of the above-mentioned Framework programme are a greater **priority for BMBF funding**, potentially leading to different national funding priorities than the ranking for EU funding. The evaluation criteria are stated in the **national calls** (see above).
  - ECS part of the Chips JU:
    - The BMBF strives to ensure high synergies between IPCEI Microelectronics & Communication Technologies and Chips JU activities. Therefore those companies and projects in the Innovation Actions of the ECS part of the Chips JU have a higher funding priority that aim for innovation beyond the R&D-topics for which they are funded already through the IPCEI
    - The focus topic IA Automotive Chiplets has the highest priority for the BMBF.
    - Potential applicants for the focus topics are urged to contact the national contact persons (see above) before the Project Outline is submitted to the Chips JU.
  - Chips for Europe Initiative part of the Chips JU:
    - How the call "Support to start-ups and SMEs making use of the Design Platform" will be supported by BMBF is to be determined.
- The BMBF funding aims at strengthening the innovation capabilities of project partners and companies located in Germany who intend to exploit research results in Germany and Europe, as well as to accelerate technology transfer into practical applications.
- Funding may be awarded for high-risk pre-competitive industry-driven research and development projects with an application-oriented approach and a high level of innovation which could not be accomplished without public funding. Projects should illustrate the added value of R&D&I results on the basis of an appropriate application, e.g. a demonstrator.
- The Project Outline (PO) and Full Project Proposal (FPP) submitted to the CHIPS JU shall include a fully completed "National Grant" table. The "National Grant" table shall include the budget (including national funding request) established according to the rules for cost eligibility and amounts applicable in Germany for purely national funding. If a single legal entity

("organisation" in Part A of the application form) requests funding for activities to be carried out at one or several organisational units ("departments") that have a high degree of autonomy and/or are located in a different *Land* from the organisation, the budget for each such department shall be listed separately in the "National Grant" table. Please refer to https://www.elektronikforschung.de/foerderung/bekanntmachungen/chipsju where a template for the "National Grant" table is available. **The eligibility of German project partners cannot be evaluated without the "National Grant" table.**

a) Consortium configuration

For proposals submitted to the ECS part of the CHIPS JU, the consortium configuration needs to fulfil the following criteria.

- To be eligible for national funding, the overall effort of any project with participants from Germany should be at least 50 person years. Additionally, German participation in this project should be at least 10% of the overall effort. Moreover, each German partner should contribute substantially to the effort of the German consortium.
- Each consortium has to reflect an appropriate balance between industrial companies, RTOs and academia: the ratio of efforts (in person months) between companies and research institutions from Germany in any given project should be 2:1 or higher.
- Germany aims at a high participation of SMEs and supports the Horizon Europe goal that a minimum of 20 % of the total public funding should be awarded to SMEs.
- If a proposal is not coordinated by a German partner, the German consortium shall appoint a contact person to the German funding authorities. This contact person has to be marked in the National Grant Table.

3. Eligibility of the costs and funding

a) Eligibility of costs

- The eligibility of costs is regulated in the BMBF's standard terms and conditions for grants on expenditure or cost basis and the administrative regulations under sections 23 and 44 of the Federal Budget Code (BHO).

b) Funding and funding rates

- Financial BMBF support is awarded in the form of project funding as non-repayable grants to participants.
- Complete information on the national application process can be found in the **national calls** "Richtlinie zur Förderung der Mikroelektronik-Forschung von Verbundpartnern im Rahmen des Gemeinsamen Unternehmens Chips" and "Richtlinie zur Förderung der Forschung zu Quantentechnologien im Rahmen des Gemeinsamen Unternehmens Chips" respecitively.

- National grant applications shall not be handed in before they are requested by the national funding authority. In case the FPP is selected to be funded nationally, the national funding authority will contact each partner individually in order to request a national grant application.
- The national funding aims at mirroring the funding which a participant actually receives from the Joint Undertaking in absolute amounts (EUR), matching up to 1:1. Funding decisions and reimbursement rates also depend on budgetary and policy considerations. The national funding may therefore be below a 1:1 ratio per partner.

Greece

GSRI – General Secretariat for Research and Innovation,

Ministry for Development

National contact person for CHIPS JU programme

Country	Name	First name	Tel	E-mail
Greece	KOTSIAS	Michael	+30 2131300102	m.kotsias@gsrt.gr
	KARAISKOU	Elisavet	+30 2131300098	e.karaiskou@gsrt.gr
	ANOUSAKI	Georgia	+30 2131300128	g.anousaki@gsrt.gr

National Funding Agency for Greece: General Secretariat for Research and Innovation (GSRI), Ministry for Development and Investments (www.gsri.gov.gr)

A. Legal requirements for the eligibility of a partner or a project

- **Type or nature of participants**

GSRI potentially supports all private and public legal entities legally operating in Greece (not natural persons) namely:

i. Research and knowledge-dissemination organizations (e.g. Higher-education Institutions or Research Centers/Institutes).

ii. Undertakings (a private and/or public sector unit, regardless of its legal status or size, engaged in economic activity).

iii. Other entities that will be considered as Research and knowledge-dissemination organizations, if respective requirements are met, or undertakings.

Besides natural persons, the following categories of undertakings are also not eligible:

- An "undertaking in difficulty" (according to art.2 of Reg. (EU) 651/2014[31]).
- An undertaking which is subject to an outstanding recovery order following a previousCommission decision declaring an aid illegal and incompatible with the internal market.

- **Legal, administrative and financial conditions**

Eligible activities

[31] Reg, (EU)651/2014 as amended by Reg.(EU) 2021/1237 & Reg.(EU) 2023/1315

- All funded activities must comply with the National RIS 3 (https://gsri.gov.gr/ethniki-stratigiki-exypnis-exeidikefsis-2021-2027/ ; https://www.espa.gr/el/Pages/RIS3.aspx).
- In case of participants falling under category (b) the main part of the project should fall within the categories of industrial research or experimental development or feasibility studies (according to the provisions of art 25 of Reg. EU 651/2014[32]). For SMEs funding for innovation activities (art. 28 of Reg. EU 651/2014[33]) may also be provided.

- **Consortium configuration:**

No restrictions.

- **Other conditions**

All applications should be accompanied by all elements and relevant documents that allow the Greek authorities to assess the eligibility criteria, and particularly those with regard to Article 2 of GBER Regulation, 651/2014 for undertakings in difficulty and the size of undertakings/enterprises.

Companies (business partner in the project) must provide specific information on the possible industrial and commercial impact of the project to the country and in Europe and justify that they have the necessary means to exploit the project results.

Following the final approval of the list of beneficiaries by the CHIPS JU, a national call will be published by GSRI. At national level, only legal and financial eligibility check is conducted and not a full peer review.

B. Eligibility of the costs and funding

- **Eligibility of costs**
  - *Double funding*

The project submitted for funding must neither have already benefited from public funding nor be redundant or overlap with projects or part of projects already funded.

  - *Co-founding source*

National Strategic Reference Framework -NSRF 2021-2027.

- ***National public funding rates***

[32] Reg, (EU)651/2014 as amended by Reg.(EU) 2021/1237 & Reg.(EU) 2023/1315
[33] Reg, (EU)651/2014 as amended by Reg.(EU) 2021/1237 & Reg.(EU) 2023/1315

Public Research Institutes and Universities: the aid intensity can reach 100% for performing non-economic activities (less the contribution of the JU) in accordance with point 19, article 2.1.1 of the «Framework for State aid for research and development and innovation» (2014/C 198/01).

Private Sector: (a) 50% of the eligible costs for industrial research; (b) 25% of the eligible costs for experimental development; (c) 50% of the eligible costs for feasibility studies.

The aid intensities for industrial research and experimental development may be increased up to a maximum aid intensity of 80 % of the eligible costs in accordance with points (a) to (d), where points (b), (c) and (d) must not be combined with each other:

(a) by 10 percentage points for medium-sized enterprises and by 20 percentage point for small enterprises;

(b) by 15% points if one of the following conditions is fulfilled:

(i) the project involves effective collaboration:

- between undertakings among which at least one is an SME, or is carried out in at least two Member States, or in a Member State and in a Contracting Party of the EEA Agreement, and no single undertaking bears more than 70 % of the eligible costs, or
- between an undertaking and one or more research and knowledge-dissemination organisations, where the latter bear at least 10 % of the eligible costs and have the right to publish their own research results;

(ii) the results of the project are widely disseminated through conferences, publication, open access repositories, or free or open source software;

(iii) the beneficiary commits to, on a timely basis, make available licences for research results of aided research and development projects, which are protected by intellectual property rights, at a market price and on non-exclusive and non-discriminatory basis for use by interested parties in the EEA;

(iv) the research and development project is carried out in an assisted region fulfilling the conditions of Article 107(3), point (a), of the Treaty;

(c) by 5 percentage points if the research and development project is carried out in an assisted region fulfilling the conditions of Article 107(3), point (c), of the Treaty;

(d) by 25 percentage points if the research and development project:

(i) has been selected by a Member State following an open call to form part of a project jointly designed by at least three Member States or contracting parties to the EEA Agreement; and

(ii) involves effective collaboration between undertakings in at least two Member States or contracting parties to the EEA Agreement when the beneficiary is a SME, or in at least three Member States or contracting parties to the EEA Agreement when the beneficiary is a large enterprise; and

(iii) if at least one the two following conditions is fulfilled:

- the results of the research and development project are widely disseminated in at least three Member States or contracting parties to the EEA Agreement through conferences, publication, open access repositories, or free or open source software; or
- the beneficiary commits to, on a timely basis, make available licences for research results of aided research and development projects, which are protected by intellectual property rights, at a market price and on non-exclusive and non-discriminatory basis for use by interested parties in the EEA."

The aid intensity for feasibility studies may be increased by 10 percentage points for medium-sized enterprises and by 20 percentage points for small enterprises.

Maximum aid intensity for undertakings is calculated according to paragraphs 5,6,7 of article 25 and art. 28 of Reg. (EU) 651/2014 (table 1).

Type of action/Type of Beneficiary	**Large enterprise**	**Medium Enterprise**	**Small Enterprises**	**Public Research Institutes and Universities**
Research and Innovation action	25-50% (-JU%)	35-60% (-JU%)	45-70% (-JU%)	100% (-JU%)
Innovation Action	50-75% (-JU%)	60-80% (-JU%)	70-80% (-JU%)	100% (-JU%)

Additional Information to be provided at submission and other conditions.

VAT eligibility: Only non-reclaimable VAT is eligible

Hungary

National contact person for Chips JU programme

Country	Name	First	Phone	email
Hungary	CSESZNOK	Flora		ncp@nkfih.gov.hu

(Web site or any other information source of the national funding authority as a reference to the applicants.)

https://nkfih.gov.hu/about-the-office

1. Legal requirements for the eligibility of a partner or a project

Legal entities established in Hungary or in the European Economic Area with a registered office and a branch in Hungary may apply for funding as follows:

a) Legal entities, non-profit-making companies and other economic entities with GFO codes 113, 114, 141, 572, 573, which meet all of the following criteria:

- have at least one closed, approved, full (365 days) fiscal year,
- maintain double-entry bookkeeping

b) Non-profit and other not-for-profit organisations with GFO codes 551, 552, 559, 562, 563, 569, 599, 931, which are designated as a state-recognised, non-state higher education institution (ecclesiastical or private higher education institution) in Annex 1 to Act CCIV of 2011 on National Higher Education and are also classified as a research and knowledge intermediary organisation4 according to Article 2, point 83 of Commission Regulation (EU) No 651/20143.

c) Bodies with GFO codes 311, 312, 322, 341, 342, 381, 382 which are classified as research and knowledge intermediary organisations according to Article 2(83) of Commission Regulation (EU) No 651/2014.

Applications for funding can be submitted individually or in the form of a national consortium of national partners in an international project. For the purposes of this Call, the applicant is understood to be the organisation implementing the project specified in the grant application on its own or, in the case of a consortium application, the leader of the research consortium organised to implement the project specified in the grant application, and the other members of the research consortium are understood to be the consortium members. The applicant and the consortium members are hereinafter referred to collectively as the applicant(s) or, in the case of a grant decision, the beneficiary(ies).

2. Eligibility of the costs and funding

g) Eligibility of costs

Amount of the grant: the maximum amount of non-repayable grant that may be requested by a national organisation submitting a grant application under this Call is the part of the grant amount in euros to be financed from national resources, as specified in the international decision taken on the basis of the international evaluation, converted into forints.

h) National public funding rates

Type of action/Type of Beneficiary	**Large enterprise**	**SME**	**Public Research Institutes and Universities**
Research and Innovation action	up to 70%	up to 80%	100%
Innovation Action	up to 50%	up to 70%	100%

i) Additional Information to be provided at submission and other conditions.

All Hungarian entities listed under Section 1. are eligible to participate in the calls. Hungarian entities that are maintained by public trusts under Act 2021/IX, thus subject to the Council Implementing Decision 2022/2506 are also eligible to participate, the EC budget share will be covered by the Hungarian Government's Guarantee Fund.

Ireland

National contact person for Chips JU programme

Country	Name	First	Phone	email
Ireland	O'Reilly	Stephen	+353879281449	Stephen.oreilly@enterprise-ireland.com

1. Legal requirements for the eligibility of a partner or a project

a) Type or nature of participants

Companies that are eligible to receive R&D funding from one of the following agencies will be considered for funding; Enterprise Ireland, IDA Ireland or Údarás na Gaeltachta.

Irish third level research performing organisations will also be considered for national funding.

It is important to note that a successful application to Chips JU does not guarantee funding by a national agency. Participants from Ireland are strongly advised to discuss applications with their national agency contact prior to submission to Chips JU

b) Legal, administrative and financial conditions

The relevant national funding agency should be satisfied that a company seeking national funding has the potential to derive a benefit, proportionate to the national funding being sought, through the exploitation of the results of the proposed project or otherwise. Companies applying for National R&D support will need to be EBITDA positive for 9 consecutive months prior to any approval. Companies that are classified as 'High Potential Start-Up' (HPSU) are not normally eligible.

All participants are advised to contact the relevant national funding agency before committing to participate in any proposal.

Higher Education Institutions will be eligible only if there is also at least one Irish based company that meets the national eligibility criteria in the consortium, and the national funding agencies are satisfied that there will be a benefit from the participation of the Higher Education

Institution, proportionate to the funding being sought, for an Irish based company or companies that the agencies are satisfied to support.

c) Consortium configuration

Projects should be introduced by companies and primarily executed to the benefit of these entities.

2. Eligibility of the costs and funding

a) National public funding rates

All Grant funding to companies is provided on a scale, depending on company size and can reach a max of 50% of eligible expenditure for Enterprise Ireland and Údarás na Gaeltachta clients. Funding available to IDA Ireland clients can vary and exact levels should be confirmed with the company contact.

Funding to 3rd level institutions is provided as a grant of 100% eligible expenditure less JU contribution up to the value of €250,000 (excluding overhead)

Type of action/Type of Beneficiary	**Large enterprise**	**SME**	**Public Research Institutes and Universities**
Research and Innovation action	Up to 30%	Up to 50%	65%
Innovation Action	Up to 30%	Up to 50%	65%

b) Additional Information to be provided at submission and other conditions.

Please note that each Irish participant must create a PDF file indicating how they meet the national eligibility criteria for funding as indicated in the Irish section of the Eligibility Criteria document published in the Call. You must upload this in the Chips JU Proposal Submission system as Part C of the Project Proposal (one file for each participant).

Note that Irish companies must clearly state in the proposal the following points:

1. From which of the three Irish agencies (Enterprise Ireland, IDA Ireland or Udaras na Gaeltachta) it is eligible to receive national R&D funding

2. Explain how it has the potential to derive a benefit, proportionate to the national funding being sought, through the exploitation of the results of the proposed project or otherwise.

Israel

Israel national contact persons for Chips JU programme

Name	First	Phone	email
Seker Loutaty Avrahami	Dan Rachel Moshe	00972527334127 00972528913774 00972545882322	Dan@iserd.org.il Rachel.l@iserd.org.il Moshe.Avrahami@innovationisrael.org.il

Web sites:

Israel Innovation Authority – Procedure 22.11.23

MAGENT CONSORTIA PROCEDURES

How to apply:

Please contact Israel Innovation Authority – ISERD for further information

1) **Legal requirements for the eligibility for national funding of a partner**

i. Israeli Corporate engaged in R&D activity for commercial purpose and meets Israel Innovation Authority regulations for funding ii. Israeli Research Institute, involved in R&D activity in cooperation with Israeli corporate as part of the consortium.

iii. Approved as a partner in the relevant consortium by an IIA research committee

2) **Legal, administrative and financial conditions**

As detailed in Procedure 22.11.23 above and inter alia:

I. Eligibility for national funding is subject to **prior local submission**, review and IIA committee decision
II. Financial conditions as per Chips-JU regulations
III. An entity may apply to Chips-JU call without requesting national funding

3) Eligibility of the costs and funding

I. Eligibility of costs

Eligible costs and expenses – in line with the CHIPS JU European rules

II. National funding rates

Type of action/Type of Beneficiary	**Large enterprise**	**SME**	**Public Research Institutes and Universities**
Research and Innovation action	Equal to the Chips-JU decision or 33% (the lowest)		Equal to the Chips-JU decision or 40% (the lowest)
Innovation Action	Equal to the Chips-JU decision or 33% (the lowest)		Equal to the Chips-JU decision or 40% (the lowest)

The IIA grant under this program is exempt from royalties.

Italy

Ministry of Enterprises and Made in Italy (MIMIT) which is committing 18 million euro as grants. MIMIT supports the calls: HORIZON-JU-Chips-2025-IA, HORIZON-JU-Chips-2025-IA FT1
The specific eligibility criteria and funding rules for each funding organization are described the following paragraphs.

Ministry of Enterprises and Made in Italy (MIMIT)

National contact person for Chips JU programme

Country	Name	First	Phone	email
Italy - MIMIT	Milazzo	Valentina		valentina.milazzo@mise.gov.it
	Lippolis	Massimiliano		massimiliano.lippolis@mise.gov.it
	Alvino	Christian		christian.alvino@mise.gov.it

Ministry of Enterprises and Made in Italy www.mimit.gov.it

1. **Legal requirements for the eligibility of a partner or a project**

a) Type or nature of participants

The following entities are eligible:

- Enterprises;

- Research Centers

- Universities and research organizations - only in collaboration with enterprises with which to set up a Consortium or a Network of Companies. The lead partner of the joint project must be an Italian enterprise.

b) Legal, administrative and financial conditions

Article 11-bis of the Decree-Law of August 9, 2024, No. 113, converted with amendments by Law No. 143 of October 7, 2024, allocated financial resources for the intervention "Partnerships for Research and Innovation - Horizon Europe" for the years 2025-2026.

The projects will be financed by respecting what is established in the Regulation (EU) GBER n.651/2014 and Regulation (EU) 2021/1237 of the Commission amending Regulation (EU) No 651/2014 declaring certain categories of aid compatible with the internal market in application of Articles 107 and 108 of the Treaty.

The projects financed by the Ministry of Enterprises and Made in Italy (MIMIT) shall comply with the acts related to the specific measure (ad hoc Ministerial Decree, and the following DGIAI Directorial Decree).

The applicants must ensure that the implementation of project activities complies with the "do no significant harm" (DNSH) principle as set out in Article 17 of Regulation (EU) 2020/852 and in accordance with the technical guidelines on the application of the principle (European Commission Communication 2021/C58/01).

The applicants are expected to comply with the principle of gender equality in relation to Articles 2, 3 (3) of the TEU, 8, 10, 19 and 157 of the TFEU, and 21 and 23 of the Charter of Fundamental Rights of the European Union, and the obligation of protection and enhancement of young people, under penalty of the possibility of suspension or revocation of the loan in the event of ascertaining the violation of these general principles.

The Ministry of Enterprises and Made in Italy (MIMIT) will exclude from funding any activity included in the Annex V, point B of the Regulation (EU) 2021/523 of the European Parliament and of the Council establishing the InvestEU programme and amending the Regulation (EU) 2015/1017.

c) Consortium configuration

The Italian consortium must include at least one Italian company. The project shall be executed primarily to the benefit of the company/es. The Ministry will apply the Virtual Common Pot by financing national applicants.

d) Other conditions

Companies must have the financial means to execute the project and a potential to use the results.

The participant should foresee, after the end of the project, the exploitation of the results of the project so to guarantee the return of the investment.

Calls supported, budget available and maximum funding per project

MIMIT committed a budget of 18 million euro as grant.

The calls supported by MIMIT, the budget tentatively allocated to each call and the maximum funding per project that can be requested by Italian participants are shown in the following table:

Call	Total budget for the call	Maximum funding per project
HORIZON-JU-Chips-2025-IA	5,000,000	3,000,000

HORIZON-JUChips-2025-IA FT1	13,000,000	13,000,000
HORIZON-JU-Chips-2025-IA-EDA	2,000,000	2,000,000

2. Eligibility of the costs and funding

a) Eligibility of costs

All costs incurred during the lifetime of a project under the following categories are eligible: personnel, equipment, subcontracting, consumables, and overheads. Overheads are calculated as a fixed percentage 25% of eligible costs of the project, as established by art. 20 of the delegated regulation (EU) n 480/2014 and by art. 29 of the regulation (EU) n. 1290/2013, in line with the provisions of art 53.3 lett. c of Regulation (EU) 1060/2021 as referred to in art. 10 paragraph 4 of Decree 121/2021. They include also communication, dissemination and travel expenses.

b) National public funding rates

Type of action/Type of Beneficiary	**Large enterprise**	**SME**	**Public Research Institutes and Universities**
Research and Innovation action	Not funded	Not funded	Not funded
Innovation Action (General) (T1)	20% 25%	30% 35%	35% 35%

c) Additional Information to be provided at submission and other conditions.

All Italian participants must submit a national application to the following email address: dgiai.div06@pec.mimit.gov.it. These documents must be submitted to MIMIT by the same deadline of the Chips JU calls *(17 September 2025, 17:00).* Any participant who does not send its national application by this deadline, will be considered ineligible.

Latvia

National contact person for Chips JU programme

Country	Name	First	Phone	email
Latvia	Sīka	Lauma	+371 67047981	lauma.sika@izm.gov.lv
Latvia	Mickeviča	Sarmīte	+371 67047984	sarmite.mickevica@izm.gov.lv
Latvia	Asmuss	Jūlija	+371 28345627	julija.asmuss@lzp.gov.lv

1. Legal requirements for the eligibility of a partner or a project

1) Type or nature of participants

Following legal persons (as defined under the Latvian law) are eligible for funding, except natural persons:

- enterprises, companies and/or industry associations, when they form part of consortia with R&D institutions;
- R&D institutions - research institutes, universities, higher education establishments, their institutes and research centres etc.

2) Legal, administrative and financial conditions

The funding of RTD activities is provided pursuant in accordance with the Regulation of the Council of Ministers of the Republic of Latvia No 259 on the procedure for providing support for participation in international cooperation programs for research and technology (adopted on 26 May 2015). This includes amendments, which include a reference to the Regulation (EU) 2021/695 of the European Parliament and of the Council of 28 April 2021 establishing Horizon Europe – the Framework Programme for Research and Innovation, laying down its rules for participation and dissemination, and repealing Regulations (EU) No 1290/2013 and (EU) No 1291/2013 (Text with EEA relevance) (OJ L 170, 12.5.2021), Council Regulation (EU) 2021/2085 of 19 November 2021 establishing the Joint Undertakings under Horizon Europe and repealing Regulations (EC) No 219/2007, (EU) No 557/2014, (EU) No 558/2014, (EU) No 559/2014, (EU) No 560/2014, (EU) No 561/2014 and (EU) No 642/2014 (OJ L 427, 30.11.2021) and European Partnerships under Horizon Europe.

R&D institution (research institutes, universities, higher education establishments, research centres etc.) must be listed in the Registry of Research Institutions operated by the Ministry of Education and Science of the Republic of Latvia.

Private entities must be registered in the Registry of Enterprises of the Republic of Latvia and provide most of its R&D&I activities in the Republic of Latvia.

The principle of forbidding double funding will be applied when granting National funding.

3) Consortium configuration

Enterprises, companies and/or industry associations participate in the projects, when they form part of consortia with Latvian R&D institutions.

If there is no Latvian enterprise involved as a partner in the project, the industrial relevance of the involvement of a R&D institution must be justified by declaration from the Latvian Information and Communications Technology Association (LIKTA) or from the Latvian Electrical Engineering and Electronics Industry Association (LEtERA) confirming the relevance of the project outcomes to the national economy, which are included as a part C of the full project proposal. If there is no research organisation involved as a partner in the project, Enterprises and industry associations must provide declaration on the possible industrial impact and justify that they have the necessary means to exploit the project results which is included as a part C of the full project proposal.

2. Eligibility of the costs and funding

1) Eligibility of costs

1. Direct costs:

1.1. Personnel costs – R&D related personnel costs should reach 80% of person/months,

1.2. Other direct costs such as consumables, equipment (only depreciation costs), materials and etc., 1.3. Subcontracts (up to 25% of total participant's direct costs),

1.4. Travels costs (up to € 18,000 per participant per project),

1.5. Project management costs,

2. Indirect costs (can reach a maximum of 25% of the total direct costs).

*2) Funding rates**

Type of activity	*Large Enterprises*	*Small and Medium Enterprises*	*Public Research Institutes and Universities*
Research and Innovation action	*up to 50%*	*up to 60%***	*up to 100%****
Innovation action	*up to 35%*	*up to 50%***	*up to 100%****

* total public funding including National and EU contribution;

** may be increased by 20%, if it is approved by National Funding Authority prior the proposal submission to Chips JU Call;

*** the aid intensity for research and development activities carried out by Public Research Institutes and Universities might be at the level of 100% only if the organisation entirely complies with the requirements set by the Commission Regulation (EU) No 651/2014 of 17 June 2014.

National funding for eligible Latvian partners is up to € 100 000 per partner, per year, per project.

Additional Information to be provided at submission and other conditions

The national funding committed for the Chips JU 2025 is EUR 1 200 000.

Lithuania

National contact person for Chips JU programme

Country	Name	First	Phone	email
Lithuania				

(*Web site or any other information source of the national funding authority as a reference to the applicants.)*

<Name of the agency/ministry> www.<xxx>.<xx>

3. Legal requirements for the eligibility of a partner or a project

a) Type or nature of participants

To be confirmed at later stages

b) Legal, administrative and financial conditions

To be confirmed at later stages

c) Consortium configuration

To be confirmed at later stages

d) Other conditions

To be confirmed at later stages

4. Eligibility of the costs and funding

a) Eligibility of costs

To be confirmed at later stages

b) National public funding rates

Type of action/Type of Beneficiary	**Large enterprise**	**SME**	**Public Research Institutes and Universities**
Research and Innovation action		40 % SME	65% RTO
Innovation Action		40 % SME	65% RTO

c) Additional Information to be provided at submission and other conditions.
The information is preliminary - subject to formal approval, budget availability and eligibility, at later stages.

Malta

National contact person for Chips JU programme

Country	Name	First	Phone	email
Malta	VASSALLO PARNIS	Josephine	+356 2542 3427	josephine.vassallo@maltaenterprise.com

Type and nature of entities that may be supported

All enterprises that are eligible to receive support from Malta Enterprise will be considered for funding.

Malta Enterprise will consider supporting academic and research organisations if they do not engage in economic activities.

Academic and research organisations are required to articulate the national industrial relevance of the project, particularly highlighting exploitation opportunities for enterprises having an operational presence in Malta.

Legal, Administrative and Financial conditions

For an enterprise to the considered for funding, it must meet the criteria established in the National Rules. The enterprise must have a permanent establishment in Malta and provide evidence to Malta Enterprise that it possesses the financial resources necessary to carry out the project.

Support to academic and research organisations will be considered if they have a permanent establishment in Malta capable of carrying out Research and Development activities.

Malta Enterprise shall require ALL applicants to demonstrate how the proposed project shall support national economic development targets.

Consortium configuration

Malta Enterprise does not impose specific consortium configuration requirements however, it may require that projects submitted by large enterprises include at least one SME with a permanent establishment in Malta or an academic or research organisation established in Malta.

Eligibility of the Costs

It is recommended that the project and its budgeted costs be discussed in advance with Malta Enterprise. For enterprises, eligible costs must be structured in accordance with the National Rules and should align with those outlined in the Grant Agreement with Chips JU, as well as with the costs reported to Chips JU.

National public funding rates

All funding to enterprises shall depend on the enterprise size and other parameters that are detailed in the National Rules. The funding rates specified hereunder reflects the total public funding allowed and hence the funding rate approved by Chips JU will have to the deducted from these percentages.

Type of Action/Type of Beneficiary	Large enterprise	SME	Public Research Institutes and Universities
Research and Innovative action	up to 50%*	up to 70%*	Up to 100%***
Innovation Action	up to 50%**	up to 50%**	Up to 100%***

* Support for enterprises shall be awarded in terms of the Research and Development - Incentive Guidelines (the National Rules).

** Support for enterprises may be provided in accordance with State Aid rules applicable to the project.

*** Funding for academic and research organisations may be provided at a rate of up to 100% provided the organisation does not carry out economic activity and meets the definition of a research and knowledge dissemination organisation as set out in the General Block Exemption Regulation (GBER).

Other conditions

Applicants seeking funding from Malta Enterprise must submit a separate request, independent of the project proposal submitted to Chips JU. All requests for national funding are to be made directly to Malta Enterprise.

Applicants will be required to describe the project's expected impact on Malta's economic development. Those intending to apply for national funding are strongly encouraged to liaise with the national contact point as early as possible.

A formal funding request must be submitted to Malta Enterprise before the project commences. If approved, applicants will be required to sign a grant agreement with Malta Enterprise in order to receive national co-funding.

Netherlands

National contact person for Chips JU programme

Country	Name	First	Phone	email
Netherlands	van der Bijl	Bob	+31 6 21839477	chipsju@rvo.nl
	de Boer	Jacob Jan	+31 6 23311252	

Background documents and other information can be downloaded from the website of Netherlands Enterprise Agency: https://www.rvo.nl/subsidies-financiering/chips-ju. The Dutch text on this website takes precedence over the English text below.

Legal requirements for the eligibility of a partner or a project

1) Admission conditions

The Netherlands will support the Dutch partners in projects selected by the Chips Joint Undertaking ECS part and Chips IA-LEAI call when:

- the project concerns industrial research, experimental development or a combination of these;
- in the project one or more Dutch partners are involved which include minimal one industrial partner. In the case of only a single Dutch partner participating in a project, it has to be an SME;
- the industrial partners of the Dutch consortium provide the major contribution to the Dutch part of the project in such a way that the major part of the public funding (Chips JU + NL) involved goes to the industrial partners of the Dutch consortium;
- the objectives of the Dutch part of the project fit within the Innovation Contract High Tech Systems and Materials (HTSM) and its underlying Roadmaps (https://hollandhightech.nl/innovatie/technologieen);
- the project complies with the “Algemene wet bestuursrecht” and the “Kaderwet EZK- en LNV-subsidies”.

Dutch partners in a proposal must include in the Project Outline (PO) sent to the Joint Undertaking the following information:

- Explanation of the contribution to the objectives of the Innovation Contract High Tech Systems and Materials (HTSM) and its underlying Roadmaps (https://hollandhightech.nl/innovatie/technologieen)

Dutch partners in a proposal must include in the Full Project Proposal (FPP) sent to the Joint Undertaking the following information:

- Authorisation form;
- Explanation of the contribution to the objectives of the Innovation Contract High Tech Systems and Materials (HTSM) and its underlying Roadmaps (https://hollandhightech.nl/innovatie/technologieen)
- Model overview of the costs.

Note that in case that there are several Dutch partners in the proposal, the Dutch partner coordinating them (the so-called "Dutch coordinator") will be in charge of submitting the above information on their behalf. The information and forms will be submitted as the **National Part** of the FPP in a ZIP file through the Chips Proposal Submission system. There will be only one ZIP file for all Dutch participants in a given proposal.

The required forms can be downloaded from the website of Netherlands Enterprise Agency: https://www.rvo.nl/subsidies-financiering/chips-ju.

2) Rejection conditions

An application for support of the share of Dutch participants of a project is rejected when:

- the partner that submits the application on behalf of all Dutch partners (the "Dutch coordinator") is not an enterprise;
- only a single Dutch partner is participating in a project that is not an SME;
- it is not credible that the Dutch partners can finance their share in the project;
- it is credible that the project would have been finished without substantial delays without subsidy;
- there is insufficient trust that Dutch partners have the necessary capacities to fulfil the project as submitted;
- the project has insufficient positive effects on the Dutch economy;
- the Dutch part of the project contributes insufficiently to the objectives of the Innovation Contract High Tech Systems and Materials (HTSM) and its underlying Roadmaps (https://hollandhightech.nl/innovatie/technologieen).

Eligibility of the costs and funding

1) Eligibility of costs

- The **eligible costs for subsidy** are in compliance with the R&D&I State Aid Rules, the “Algemene wet bestuursrecht” and the “Kaderwet EZK- en LNV-subsidies”.
- The Dutch subsidy percentages are indicated below in the section Funding Rates.
- In case another Dutch administrative body has already granted a subsidy for the eligible costs of the Dutch part of an Chips project or part of such project, the contribution by the Ministry of Economic Affairs will be granted so that the total amount of subsidy will not exceed the before-mentioned Dutch subsidy percentages.

- In case that a contribution has been already granted for the eligible costs for subsidy to the Dutch part of an Chips project or part of it on the basis of a subsidy scheme of the Ministry of Economic Affairs, no additional subsidy will be granted by the Ministry of Economic Affairs for the already subsidized part.
- Per individual Dutch partner the subsidy percentages will be applied according to the activities. The project eligible costs per partner will be defined and the corresponding percentages will be applied.
- Per Chips JU ECS project or Chips IA-LEAI project in which a Dutch consortium takes part a total national maximum of € 5.000.000 funding for the Dutch consortium will be initially applied.
- The Dutch budget for the Chips JU ECS and Chips IA-LEAI Calls 2025 is in total € 25.150.000 (subject to parliamentary approval) and will initially be split as follows:
    - A joint budget for the focus topics HORIZON-Chips-2025-IA FT1, HORIZON-Chips-2025-IA FT2 of € 3.160.000
    - A budget for the call HORIZON-Chips-2025-IA HIA of € 1.000.000.
    - A joint budget for the global calls HORIZON-JU-Chips-2025-IA and HORIZON-Chips-2025-RIA is € 20.000.000.
    - A budget for the call DIGITAL-Chips-2025-1-IA-LEAI of € 990.000.
- RVO (Netherlands Enterprise Agency) will be in charge of the project administration of all projects of the Chips JU Calls.

2) National public funding rates

Type of action/Type of Beneficiary	**Large enterprise**	**SME**	**Public Research Institutes and Universities**
Research and Innovation action	20%	30%	25%
Innovation Action	20%	30%	25%

In case the EU funding rates and/or conditions are modified the national funding rates may be amended.

Norway

National contact point

Country	Name	First name	Tel	E-mail
Norway	Liv	Furuberg	(+47) 93059326	Lfu@rcn.no
Norway	Waqar	Ahmed	(+47) 47297558	wah@rcn.no

The Research Council of Norway

Applicants are advised to consult the national contact point for a pre-eligibility check

ECS CALLS

1. Legal requirements for the eligibility of a partner or a project

1.1. Type or nature of participants (project partners)

a) Norwegian companies: Commercial enterprises registered in Norway in The Register of Business Enterprises.
b) Norwegian research organisations approved by the Research Council of Norway. Approved research organisations (forskningsradet.no)

1.2. Legal, administrative, and financial conditions

a) General eligibility criteria and conditions for receiving project funding from the Research Council of Norway will apply (i.e., the beneficiary must be a registered legal entity, have credible capacity to execute the project activities, demonstrate financial viability, and provide transparency as to funding requested or received from other sources).
b) Companies must be established with a considerable business activity in Norway within the scope of the Chips JU project.
c) All project partners must possess relevant research & technology development capabilities.

1.3. Consortium configuration

a) At least one Norwegian company must be involved as a partner in the project.
b) For Research and Innovation Actions (RIAs) at least 30 % of the efforts (eligible costs) of Norwegian partners in the project must be from business partners.
c) For Innovation Actions (IAs) at least 50 % of the efforts (eligible costs) of Norwegian partners in the project must be from business partners.
d) In case of equal score, national co-funding priority will be given to a project with company partners that are new to Chips JU including its predecessor KDT JU.
e) The industrial relevance of the participation of a research organisation must be justified by declarations from the Norwegian company partner(s) in the project.
f) Companies must provide specific information on the possible industrial and commercial impact of the project and justify that they have the necessary means to exploit the project results.
g) Research organisations must specify national industrial impact in terms of exploitation opportunities for Norwegian companies.

2. Eligibility of the costs, national budget and funding rates

2.1. Eligible costs

a) Horizon Europe rules and guidelines on eligible costs will apply.

2.2. Budget

a) The total 2025 Norwegian funding budget for the Chips JU Calls is NOK 31,000,000.
b) The budget is exclusive for the non-initiative (previous KDT) part of the 2025 Chip JU work programme. There is no pre-allocated distribution of the Norwegian funding budget between the Calls in the work programme.
c) Norwegian applicants should consider NOK 11,000,000 as a maximum amount of national co-funding for one single project. In case of a single Norwegian participant, the maximum national co-funding can be NOK 4,000,000. In case if the project is coordinated by a Norwegian participant, the maximum national co-funding can be NOK 15,000,000.
d) For the project budgeting at application stage, use the NOK/€ conversation rate from a specified date close to the call deadline.

2.3. National public funding rates

a) The maximum funding rates for the national co-funding provided by the Research Council of Norway will be as listed in the table below.

Action	Large enterprises	SMEs	Research organisations
All Types	25 %	35 %	65 %

b) National co-funding will be subject to conditions in current state aid rules. See more details at: State aid (forskningsradet.no).

3. National part to be submitted as an annex to the application

Information providing the justifications required according to the requirements above must be provided as a separate attachment named "National Part" in the proposal submission tool, both at the Proposal Outline (PO) and at the Full Project Proposal (FPP) submission stage.

Information necessary to confirm whether eligibility criteria mentioned in item 2) above are fulfilled shall be submitted to the Research Council of Norway on request, before a National Grant Agreement can be established.

HORIZON-JU-Chips-2025-SGA-QAC1-2: Supporting developing Quantum Chip Technology for photonic stability Pilot.

1. Legal requirements for the eligibility of a partner or a project

1.1. Type or nature of participants (project partners)

a) Norwegian research organisations approved by the Research Council of Norway. Approved research organisations (forskningsradet.no)

1.2. Legal, administrative, and financial conditions

a) General eligibility criteria and conditions for receiving project funding from the Research Council of Norway will apply (i.e., the beneficiary must be a registered legal entity, have credible capacity to execute the project activities, demonstrate financial viability, and provide transparency as to funding requested or received from other sources).

b) All project partners must possess relevant research & technology development capabilities.

2. Eligibility of the costs, national budget and funding rates

2.1. Eligible costs

a) Horizon Europe rules and guidelines on eligible costs will apply.

2.2. Budget

a) The total 2025 Norwegian funding budget for the Chips Quantum pilot line Quantum Calls is EUR 2,000,000.

b) The budget is exclusive for the SGA quantum chip pilot line of the 2025 Chip JU work programme and the call

c) Norwegian applicants should consider EUR 2,000,000 as a maximum amount of national co-funding for one single project.

2.3. Infrastructure

a) Parts of the national funding may be used to finance research infrastructure. In that case, the RCN requirements for "research infrastructures of national importance" must be followed. The infrastructure must be made available to relevant research groups and industries.

b) National co-funding will be subject to conditions in current state aid rules. See more details at: State aid (forskningsradet.no).

3. National part to be submitted as an annex to the application

Not Applicable

Poland

National contact person for Chips JU programme

Country	Name	First	Phone	email
Poland	Nowak	Paulina	T: +48 22 25 66 735 M: +48 502 052 237	paulina.nowak@ncbr.gov.pl

(Web site or any other information source of the national funding authority as a reference to the applicants.)

National Centre for Research and Development: https://www.gov.pl/web/ncbr

Legal requirements for the eligibility of a partner or a project

a) Type or nature of participants

- Research organizations;
- Micro, Small, Medium and Large Enterprises;
- Groups of entities consisting of research and knowledge organisations/entrepreneurs (in any configuration).

b) Legal, administrative and financial conditions

All proposals must be aligned with National regulations, inter alia:

1. The Act of 20 July 2018 on the Law of Higher Education and Science, published in Journal of Laws item 742, 2023, as amended;
2. The Act of 30 April 2010 on the National Centre for Research and Development, published in Journal of Laws item 2279, 2022;
3. The Regulation of the Minister of Science and Higher Education of 19 August 2020 on granting state aid by the National Centre for Research and Development, published in Journal of Laws item 1456, 2020, as amended.

c) Consortium configuration

Groups of entities consisting of research and knowledge organisations/entrepreneurs (in any configuration).

d) Other conditions

For entrepreneurs independently undertaking projects at the national level, there is no possibility of increasing the intensity of state aid for industrial research and experimental development based on the condition of effective cooperation between entrepreneurs or between entrepreneurs and research organisations.

Eligibility of the costs and funding

a) Eligibility of costs

A detailed information (in Polish) will be available for applicants at COMPETITION PLATFORM when the call is published.

The costs eligible for funding or state aid in the case of basic research, applied research and experimental development are the costs included in the **Cost Eligibility Guide**, which is an annex to the NCBR call announcement.

Activities related to project promotion and project management cannot be a separate package work (WP/task). Costs related to these activities may be included in the WP/tasks research.

The eligible costs shall be the following:

1. **personnel costs** (researchers, technicians and other supporting staff employed on the research project);

2. **costs of subcontracting, costs of consultancy and equivalent services** used exclusively for the research activity; this cost category shall not exceed 70% of all eligible costs of a project; subcontracting a consortium partner is allowed only in justified cases, which shall be verified by a national panel of experts

3. **operating costs including** (depending on the type of eligible institution):

Research Organisations:

Costs of instruments and equipment, technical knowledge and patents are eligible only to the extent and for the period when they are used for the research project; if such instruments or pieces of equipment are not used for their entire useful life within the research project, only the depreciation costs corresponding to the life of the research project, as calculated on the basis of good accounting practice, shall be considered eligible;

• costs for buildings and land, to the extent and for the period when they are used for the research project; with regard to buildings, only the depreciation costs corresponding to the life of the research project, as calculated on the basis of good accounting practice shall be considered eligible; for land, costs of commercial transfer or actually incurred capital costs shall be eligible;

• other operating costs including: costs of materials, supplies and similar products incurred directly as a result of the research activity; training costs; travel costs including conference fees; cost of required external audit, costs of project promotion (e.g. articles, project webpage);

Enterprises:

• costs of instruments and equipment, technical knowledge and patents to the extent and for the period when they are used for the research project; if such instruments or pieces of equipment are not used for their entire useful life within the research project, only the depreciation costs corresponding to the life of the research project, as calculated on the basis of good accounting practice, shall be considered eligible;

• costs for buildings and land, to the extent and for the period when they are used for the research project; with regard to buildings, only the depreciation costs corresponding to the life of the research project, as calculated on the basis of good accounting practice shall be considered eligible; for land, costs of commercial transfer or actually incurred capital costs shall be eligible.

4. **additional overheads** incurred indirectly as a result of the research project (depending on the type of eligible institution);

Research Organisations:

additional overheads for research organizations should account 25% of all eligible direct costs; That costs (4) are counted as a multiplication by percentage given above (called x%) and the rest of direct costs for research organizations, excluding subcontracting (2); It means 4=(1+3)*25%.

Enterprises:

additional overheads for enterprises include also other operating costs, e.g. costs of materials, supplies and similar products incurred directly as a result of the research activity, training costs; travel costs including conference fees; cost of required external audit, costs of project promotion (e.g. articles, project webpage). That costs should account 20% of all eligible direct project costs; Additional overheads (4) are counted as a multiplication by percentage given above (called x%) and the rest of direct costs for enterprises; It means 4=(1+2+3)*20%.

Projects requesting more than PLN 3 million funding are entitled to claim the cost of the audit. For more details on eligible costs, applicants are advised to check the

guidelines in the call announcement on NCBR webpage.

b) National public funding rates

Funding quota of Polish participants can be up to 100% for research organisations. In the case of enterprises, funding quota will be decided on a case-by-case basis depending on the size of the company, type of research/development, risk associated with the research activities and commercial perspective of exploitation. Funding quota of Polish participants apply to Research and Innovation Action and Innovation Action. Organization must be registered in Poland.

	Large Enterprises	**Medium Enterprises**	**Micro/Small Enterprises**	**Research organization**
Fundamental/Basic Research	0%	0%	0%	0%
Industrial/Applied Research	Up to 50+5/15/25 (max 75%)	Up to 50+10+5/15/25 (max 80%)	Up to 50+20+5/15/25 (max 80%)	Up to 100%
Experimental Development	Up to 25+5/15/25 (max 50%)	Up to 25+10+5/15/25 (max 60%)	Up to 25+20+5/15/25 (max 70%)	Up to 100%

c) Additional Information to be provided at submission and other conditions.

National phase of application procedure

After international evaluation has been completed and the ranking list established, Polish participants from consortia recommended for funding will be invited to submit the National Application Form (NAF). All eligible entities invited to submit the NAF are obliged to use the rate of exchange of the European Central Bank of the day of call opening (published on the call announcement).

The Director of the National Centre for Research and Development subsequently issues a funding decision and signs national grant agreements with Polish participants providing that they have signed Chips JU grant agreements first.

Partner Search Tool

We encourage you to learn about and use our "PartFinder" (Partner Search Tool), which allows you to match science and industry entities from around the World with each other. The search tool is available at: https://partfinder.ncbr.gov.pl/.

Portugal - Agência Nacional de Inovação

National contact person for Chips JU programme

Country	Name	First	Phone	email
Portugal	Duarte	Afonso	-----	Afonso.duarte@ani.pt
	Azevedo	Sofia	-----	Sofia.azevedo@ani.pt

Agência Nacional de Inovação, S.A. (*ANI*)
Ministry of Education, Science and Innovation and Ministry of Economy and Territorial Cohesion
www.ani.pt

The National Strategy for Semiconductors (Council of Ministers Resolution 12/2024) aims to boost the microelectronics and semiconductor industry in Portugal. This will be achieved through the establishment of mechanisms that strengthen business capacity and national research and development, as well as the promotion of synergies with international partners and participation in sector-specific European programs. This strategy aligns with the Integrated Circuits Regulation (European Chips Act), which primarily seeks to invigorate Europe's capabilities in this area, spanning chip design, production, and assembly, along with the training of professionals in these fields. This aims to reverse the gradual decline in Europe's market share within the semiconductor sector.

This resolution, to be further densified through an order (*portaria*), to be approved by the government in Q3 2025, establishes the framework for allocating national support for co-financing projects falling under Pillar 1, known as the Initiative (or CHIPS for Europe), of the Integrated Circuits Regulation (European Chips Act). For the Initiative part of work programme 2025, a total amount of 6.000.000 Euro is committed to co-fund Portuguese beneficiaries covering all topics from the Initiative calls.

Except for non-profit legal entities, the national co-funding must also comply with State aid rules, specifically when granted to entities that develop an economic activity.

In this setting the General Block Exemption Regulation (Regulation (EU) 651/2014) (GBER) shall be activated by Portuguese authorities, with the potential application, conditions met and as deemed required, of the subsequent aid categories to beneficiaries that perform an economic activity, albeit with a particular focus on GBER Article 25c as we are before European R&D initiatives:

— Article 25, Aid for research and development projects;

— Article 25c, Aid involved in co-funded research and development projects;

— Article 26, Investment aid for research infrastructures; and

— Article 26a, Investment aid for testing and experimentation infrastructures.

The potential application of the *De Minimis* regulation (Regulation (EU) 2023/2831) is also foreseen.

1. Legal requirements for the eligibility of a partner or a project

All proposals must include at least one Portuguese organization, these can be:
a) Companies of any nature and under any legal form that operate within the national territory;
b) Non-business entities within the research and innovation system (ENESII), or other public and private non-profit institutions, that develop, promote, or, through effective participation, conduct scientific research and technological development activities, and operate within the national territory.

2. Eligibility of the costs and funding

a) Eligibility of costs

As a rule, eligible expenses include those defined in the European programs that will fund the CHIPS JU specifically the Chips for Europe (Initiative) calls, in articulation, when legally required, with the relevant eligibility provisions of the GBER, as detailed in TABLE 1, infra. Particular focus may be given to GEBR's Article 25c (Aid involved in co-funded research and development projects), as these are European based R&D projects.

b) National public funding rates

In the case of non-profit legal entities, the maximum funding is up to **100% of the relevant eligible costs**. For profit legal entities (SMEs and large companies), and for the purpose of determining the applicable national co-funding rates, Article 25c GBER shall apply to grants awarded under Horizon Europe, whereas Article 25 shall apply to grants awarded under the Digital Europe Programme (DEP). The maximum national co-funding rates for Portuguese undertakings in articulation with the applicable aid categories are described in TABLE 1 below.

Table 1 – Eligible costs and funding rates	
Aid category	**Maximum funding rates**
Research and Development Projects (GBER, Article 25)	Rates of support: **100% Fundamental research**. **50% industrial research.** **25% experimental development**. Increases possible for industrial research and experimental development, in accordance with Article 25(6) of the GBER, up to a maximum of 80%: Medium-sized enterprises **10%**; Small companies **20%**. These increases may be cumulative with a **15%** increase in cases of: Effective collaboration, or Wide dissemination, or Availability of licences for the project results, or If the investment is made in assisted regions that meet the conditions of Article 107(3)(a) TFEU (abnormally low standard of living or serious unemployment, regions under Article 349 TFEU). **5%** increase if the project is carried out in assisted regions that meet the conditions of Article 107(3)(c) TFEU (where they do not adversely affect trading conditions to an extent contrary to the common interest). **25%** increase if the project has been designed by several Member States or parties to the EEA Agreement (in accordance with Article 25(6)(d) of the GBER). Support rate: **50%** for feasibility studies. Increases: Medium-sized enterprises **10%** and micro and small enterprises **20%**.
Aid included in co-financed research and development projects (GBER, Article 25c)	The categories, maximum amounts and methods of calculation of the eligible costs of the action are those defined as eligible under the rules of Horizon Europe programme. Article 34 (Funding rates) of the Horizon Europe Regulation provides in this context that a single funding rate per action shall apply for all activities it funds. The maximum rate per action shall be fixed in the work programme. Up to **100%** of total eligible costs of an action under the programme may be reimbursed, except for: (a) innovation actions were, up to 70% of the total eligible costs may be reimbursed, except for non-profit legal entities where up to 100% of the total eligible costs may be reimbursed.
Research Infrastructure (GBER, Article 26)	Maximum support rate: **50%**. May be increased up to **60**% provided that at least two Member States grant public funding, or a research infrastructure is evaluated and selected at European Union level.

Testing and experimentation infrastructure (GBER, Article 26a)	Base rate: **25%** Increases up to a maximum aid intensity of **40%**, **50%** and **60%** of the eligible investment costs of large, medium-sized and small enterprises, respectively, as provided in the GBER.
De minimis aid [Regulation (EU) 2023/2831]	Other costs not financed under the above-mentioned categories of aid under the GBER. Maximum limit of € 300,000.00 over 3 years per single company.

c) Additional Information to be provided at submission and other conditions.

Once projects are approved and grants agreements signed with the CHIPS JU, the Portuguese entities benefiting from them will be invited by ANI – under objective, non-discriminatory and transparent conditions –, to submit their national grant application.

This grant application is for the purpose of allocating the national co-funding, under the terms and conditions to be defined in the national call or invite for application.

Portugal - Fundação para a Ciência e a Tecnologia

National contact person for Chips JU programme

Country	Name	First	Phone	email
Portugal	Coelho	Filipa	+351 213924450	filipa.coelho@fct.pt

Foundation for Science and Technology/ Ministry of Education, Science and Innovation

https://www.fct.pt/

For the ECS R&I part of the Work Programme 2025, a total amount of up to **3 500 000 Euro** from state budget is committed to co-fund Portuguese beneficiaries covering all topics under calls HORIZON-JU-Chips-2025-IA and HORIZON-JU-Chips 2025-RIA. The total national co-funding amount of each national beneficiary in each project cannot exceed **250 000 Euro**.

National co-funding is compatible with the internal market in the sense of article 107, paragraph 3, of the Treaty of Functioning of the European Union, being for that reason exempt from the obligation of notification foreseen in article 108, paragraph 3, of the referred Treaty, since it fulfils the conditions established in article 25-C and chapter I of the Regulation (EU) 2014/651 of the Commission of 17 June 2014.

The eligibility rules of Horizon Europe Regulation (EU) 2021/695 apply to Portuguese participation in the Chips JU 2025 R&I calls for proposals ("ECS" part), with the exceptions indicated below.

Legal requirements for the eligibility of a partner or a project

All proposals with national applicants **must include at least one Portuguese company** (large company or SME). Consortia consisting solely of non-entrepreneurial entities of the national research and innovation system (ENESII – "*entidades não-empresariais do sistema nacional de I&I*"), also designated as RTO, will not be considered eligible for Portuguese co-funding.

Funding rates

Maximum national co-funding rates for Portuguese applicants are described in the table below.

Maximum national co-funding rates			
Type of action / Type of entity	Large company	SME	RTO/ENESII
Innovation Actions	**30%**	**25%**	**65%**
Research and Innovation Actions	**25%**	**30%**	**65%**

Eligibility of the costs

Cost eligibility applicable to national co-funding will be determined based on Horizon Europe (Regulation (EU) 2021/695).

Additional Information to be provided at submission and other conditions

National participants in selected proposals will have to sign a national grant agreement ("*Termo de Aceitação*") with FCT in order to receive national co-funding.

Romania

National contact person for Chips JU programme

Country	Name	First	Phone	email
ROMANIA	ANANIA	CRISTINA	+40722 238 877 +32492 922 349	cristina.anania@mcid.gov.ro
	DINU	ELENA	+ 40.21.303.21.23/ 416	elena.dinu@mcid.gov.ro

RDI national funding Programmes

I. ***PNCDI IV - Programme 5.8.1 - European and International Cooperation, Partnerships and European Missions:*** *https://uefiscdi.gov.ro/pncdi-iv-program-8*

Institutions in charge:

I. **National Authority for Research: https://www.research.gov.ro/**
II. **Executive Agency for Higher Education, Research, Development and Innovation Funding (UEFISCDI): https://uefiscdi.gov.ro/?we=module.org.uefiscdi.home&wtok=&wtkps=TYxLEoIwEETvkrXgJAESh41HsMoTAIkxJb+CBCwp7m5AF+x65nW/AlNcRuRIRqtIPmLKkKStSD5loYRrtH+VzmTUwBN0fXnPgxfV1DLoaaR9aWQXGTPprN22YTrrLfCQmk75WsfdYGKvH3aslI0nq+e4GJytunrrUSR27yOhifwrro7kRUDLzpvjEcoWJYVLvq7hIZAo1be3+5kLYJJJSH8Suvmo5MBAwukI1y8=&wchk=4764e818dd96d739de369aefd03761e4e7505fb7**

1. Legal requirements for the eligibility of a partner or a project

a) Type or nature of participants

- National research and development institutes;
- Research institutes, centers, or stations of the Romanian Academy, as well as research and development institutes of branch academies;
- Accredited higher education institutes or their constituent structures;
- Research and development institutes or centers organized within national companies, national corporations, and autonomous administrations of national interest.

b) Legal, administrative and financial conditions

Research and innovation projects, both RIA (Research and Innovation Actions) and IA (Innovation Actions), from research organizations and the business sector, selected for funding by Chips Joint Undertaking under the Horizon Europe Programme.

PNCDI IV - Programme 5.8.1

- The funds allocated from the State Budget for Romanian partners in an Institutionalized Partnership are capped at 2,000,000 EUR per project, but not more than 1,500,000 EUR/Romanian partner.
- Call duration: February 8, 2024 – December 31, 2027.

c) Consortium configuration

Romanian partners are allowed to participate in projects either individually or as part of a consortium, as follows:

PNCDI IV - Programme 5.8.1

- An institution may participate in competitions as a project coordinator, project partner, or affiliated institution. Furthermore, an institution may take part in the national competition organized within a Partnership either as the sole Romanian partner or in collaboration with other Romanian institutions.

d) Other conditions

2. Eligibility of the costs and funding

a) Eligibility of costs

The level of funding is determined based on the types of activities and the category of institution, in accordance with the State Aid scheme – Commission Regulation (EU) No 651/2014 (Order 21324/02.11.2023 & Order 20396/06.02.2024).

i. PNCDI IV - Programme 5.8.1

(a) Direct costs:

- Personnel costs.
- Logistics:
  - Other direct costs such as consumables, and similar products necessary for research activities according to current legislation
  - Capital expenditures (for public research organizations that are not beneficiaries of state aid, 100% of the costs of equipment purchased during the project implementation period are funded. For institutions benefiting from state aid only depreciation costs). Capital expenditures cannot exceed 30% of the funding amount from the National budget
- Subcontracts (up to 25% of the funding amount from the National budget)
- Travels costs.

(b) Indirect costs (can reach a maximum of 25% of the total direct costs, excluding capital expenditures and expenses incurred by third parties).

b) National public funding rates

PNCDI IV - Programme 5.8.1

Type of action/Type of Beneficiary	**Large enterprise**	**Medium enterprises**	**SME**	**Public Research Institutes and Universities**
Research and Innovation action	Up to 65%	Up to 75%	Up to 80%	Up to 100%
Innovation Action	Up to 25%	Up to 35%	Up to 45%	Up to 100%

The maximum aid intensities granted through this scheme range from a minimum of 25% to a maximum of 80% of the total eligible project cost, as follows:

(a) 100% of eligible costs for fundamental research;
(b) 50% of eligible costs for industrial research;
(c) 25% of eligible costs for experimental development;
(d) 50% of eligible costs for feasibility studies.

The aid intensities for industrial research and experimental development can be increased:

(a) by 10 percentage points for medium-sized enterprises and by 20 percentage point for small enterprises;
(b) by 15 percentage points if one of the following conditions is fulfilled:
(i) the project involves effective collaboration:
— between undertakings among which at least one is an SME, or is carried out in at least two Member States, or in a Member State and in a Contracting Party of the EEA Agreement, and no single undertaking bears more than 70 % of the eligible costs, or
— between an undertaking and one or more research and knowledge-dissemination organisations, where the latter bear at least 10 % of the eligible costs and have the right to publish their own research results;
(ii) the results of the project are widely disseminated through conferences, publication, open access repositories, or free or open source software;
(iii) the beneficiary commits to, on a timely basis, make available licences for research results of aided research and development projects, which are protected by intellectual property rights, at a market price and on non-exclusive and non-discriminatory basis for use by interested parties in the EEA;
(iv) the research and development project is carried out in an assisted region fulfilling the conditions of Article 107(3), point (a), of the Treaty;
(c) by 5 percentage points if the research and development project is carried out in an assisted region fulfilling the conditions of Article 107(3), point (c), of the Treaty;
(d) by 25 percentage points if the research and development project:
(i) has been selected by a Member State following an open call to form part of a project jointly designed by at least three Member States or contracting parties to the EEA Agreement; and

(ii) involves effective collaboration between undertakings in at least two Member States or contracting parties to the EEA Agreement when the beneficiary is a SME, or in at least three Member States or contracting parties to the EEA Agreement when the beneficiary is a large enterprise; and

(iii) if at least one the two following conditions is fulfilled:

— the results of the research and development project are widely disseminated in at least three Member States or contracting parties to the EEA Agreement through conferences, publication, open access repositories, or free or open source software; or

— the beneficiary commits to, on a timely basis, make available licences for research results of aided research and development projects, which are protected by intellectual property rights, at a market price and on non-exclusive and non-discriminatory basis for use by interested parties in the EEA.

The aid intensities for feasibility studies may be increased by 10 percentage points for medium-sized enterprises and by 20 percentage points for small enterprises.

c) Additional Information to be provided at submission and other conditions.

Slovakia

National contact person for Chips JU programme

Country	Name	First	Phone	email
Slovakia	Kontrík	Martin	-	martin.kontrik@minedu.sk

1. Legal requirements for the eligibility of a partner or a project

a) Type or nature of participants

SME, large enterprise, University, Research institution registered in the Slovak Republic are eligible.

b) Legal, administrative and financial conditions

The national co-funding of CHIPS JU projects is provided according to:

- The Act No 172/2005 Coll. On the Organization of State Research and Development Support and Supplementation of Certain Acts
- The Act No 523/2004 Coll. on the budgetary rules of public administration and Supplementation of Certain Acts
- Community Framework for State Aid for Research and Development and Innovation (2006/C323/01)
- Eligible to ask for national co-funding is an R&D organization from every sector according to §7 of Act No 172/2005 Coll. And legal entity to §2 art. 2 of the Slovak Code of Commerce.

c) Consortium configuration

Slovak partners are allowed to participate in project alone or in cluster.

d) Other conditions

-

2. Eligibility of the costs and funding

a) Eligibility of costs

all personal costs, material costs, services, travel expenses, equipment amortization costs, indirect costs related to project solution within a period of project duration.

b) National public funding rates

Type of action/Type of Beneficiary	**Large enterprise**	**SME**	**Public Research Institutes and Universities**
Research and Innovation action	50%	70%	100%
Innovation Action	40%	60%	100%

c) Additional Information to be provided at submission and other conditions.

The proposed projects should be within the scope of the national RIS3 initiative.

Slovenia

National contact person for Chips JU programme

Country	Name	First	Phone	email
Slovenia	Kern	Špela	+386 40273392	spela.kern@gov.si

The National Funding Authority (NFA) of Slovenia is the Ministry of Digital Transformation (https://www.gov.si/en/state-authorities/ministries/ministry-of-digital-transformation/).

1. Legal requirements for the eligibility of a partner or a project

a) Type or nature of participants

SMEs, LE, research organisations.

b) Legal, administrative, and financial conditions

Following the publication of the Chips JU call, the Ministry issued an invitation for applicants to submit their requests for a letter of support by 1 September at 14:00. Applicants were required to complete a form providing basic information about the applicant, the project, and the potential financing. The Ministry subsequently issued letters of support. Those selected by Chips JU will receive national co-financing, as previously committed. The legal basis for this procedure is the Act on the Support Environment (ZPOP), the Ministry's Programme of Measures, and the strategic document Digital Slovenia 2030.

c) Consortium configuration

Consortia were established on the initiative of the applicants without the involvement of the Ministry.

d) Other conditions

Not Applicable.

2. Eligibility of the costs and funding

a) Eligibility of costs

Following types of costs are covered by national funding:

- Personnel costs Subcontractor costs
- Procurement costs
- Other costs
- Indirect costs.

b) National public funding rates

Type of action/Type of Beneficiary	**Large enterprise**	**SME**	**Public Research Institutes and Universities**
Research and Innovation action	25%	35%	35%
Innovation Action	20%	30%	35%
Simple Grants	-	-	-

c) Additional Information to be provided at submission and other conditions.

Not Applicable.

Spain

Two funding organizations will grant funding to Spanish applicants for the **Chips JU- ECS R&I 2025** and **Chips for Europe 2025** calls:

1. The Ministry for Digital Transformation and Civil Service (MTDFP) will support private companies and other private agents.

2. The Agencia Estatal de Investigación (AEI, State Research Agency) depending on the Ministry of Science and Innovation and Universities (MCIU) will support research centers, universities and non-profit private research entities.

Each Spanish participant in a **Chips JU** Consortium must request the national funding from the relevant funding entity at a later stage, in case the project is approved.

All possible applicants are strongly encouraged to inform the national contact person at the beginning of the proposal preparation process.

National contact persons for Chips JU Programme

Country	Name	Tel	E-mail
SPAIN	MTDFP: Jesús Marcos Morell Sonia Juan Vindel Álvaro Pereda Arce Guillermo Gómez Fontecha David de Francisco Marcos Juan Miguel Ibáñez de Aldecoa Quintana		chipsju@digital.gob.es
	AEI: Beatriz Gómez Miguel	+34 916038947	beatriz.gomez@aei.gob.es
	CDTI Enrique Pelayo	+34 915815566	enrique.pelayo@cdti.es

Shared conditions between the MTDFP and AEI

In order to apply for public grants, it will be mandatory to fulfil all current European legal requirements.:

- Framework for State aid for research and development and innovation (OJ 2014/C198/01).
- Council Regulation (EU) 2021/2085 of 19 November 2021 establishing Joint Undertakings under Horizon Europe (Single Basic Act) and its amending Council Regulation (EU) 2023/1782 of 25 July 2023
- Applicable rules or regulations governing the Chips JU and its 2023-2027 Multiannual Work Program including Appendix 5
- Commission Regulation (EU) No 651/2014 of 17 June 2014 declaring certain categories of aid compatible with the internal market in application of Articles 107 and 108 of the Treaty Text (GBER), when applicable.

Furthermore, with regard to any aspect not covered by European regulations, all other applicable legal requirements set out in the Spanish legal framework shall apply, for example:

- Ley 38/2003, de 17 de noviembre, General de Subvenciones.
- Real Decreto 887/2006, de 21 de julio, por el que se aprueba el Reglamento de la Ley 38/2003, de 17 de noviembre, General de Subvenciones.
- Leyes anuales de Presupuestos Generales del Estado.
- Ley 47/2003, de 26 de noviembre, General Presupuestaria.
- Ley 39/2015, de 1 de octubre, del Procedimiento Administrativo Común de las Administraciones Públicas.
- Ley 40/2015, de 1 de octubre, de Régimen Jurídico del Sector Público.
- Ley 9/2017, de 30 de octubre, de Contratos del Sector Público.
- Ley 14/2011 de 1 de junio, de la Ciencia, Tecnología e Innovación
- Ley 28/2022, de 21 de diciembre, de fomento del ecosistema de las empresas emergentes,
- Ley Orgánica 2/2023, de 22 de marzo, del Sistema Universitario.

The Spanish legal texts can be found on http://www.boe.es

MTDFP

Requirements by the Ministry for Digital Transformation and Civil Service

Legal requirements for the eligibility of a partner or a project

1) Type or nature of participants

The Ministry for Digital Transformation and Civil Service (**MTDFP**) is the national authority responsible for funding the following participants' Chips JU calls:

- Spanish enterprises (SME, LE, GE[34], RDL 1/2010, de 2 de julio, Texto refundido de la Ley de Sociedades de Capital)
- Private Technology Centres (TC, RD 2093/2008 29th December)
- Private Universities (LOSU 2/2023)

According to the Spanish Regulation, enterprises and Technology Centres (RD 2093/2008 29th December) should follow the rules and procedures for loans and grants.

Also, the Ministry for Digital Transformation and Civil Service (**MTDFP**) will also fund non-profit R&D organizations in the following calls:

- HORIZON-JU-CHIPS-2025-QAC-SGA

2) Legal and administrative requirements

Every national participant should be established in Spain, satisfy the Art. 13 of Ley 38/2003, de 17 de noviembre, General de Subvenciones (LGS) and must not be in bankruptcy or have requested bankruptcy proceedings.

[34] Group of Enterprises

For that reason, every national participant should sign a Statement of Compliance.

Therefore, every national participant should authorize the access and consultation of tax obligations, Social Security payments, fiscal residence, and Full Statement of National Insurance contributions of the workers assigned to the project and/or the verification of any other data provide during the granting and monitoring of the aid. In case the participant does not authorize the consultation, the participant shall submit the corresponding documentation.

At the Project Outline (PO) stage, the following documentation shall be submitted to the Chips JU:

- Part C (one per project, sent by the coordinator of the national sub-consortium)

Regarding the Full Project proposal (FPP) stage, the following documentation shall be submitted to the Chips JU:

- Part C (one per project, sent by the coordinator of the national sub-consortium).

Templates for the aforementioned documents will be available at the website of the Secretariat of State for Telecommunications and Digital Infrastructures or upon request.

3) Legal and administrative procedures

After signing the Grant Agreement, MTDFP will contact every beneficiary to assist in the fulfillment of forms and documents requested by the Spanish Public Authorities, to sign the National Grant Agreement document.

Payment of the national contribution will proceed regarding national rules in force.

A payment in advance is carried out after the establishment of the National Grant Agreement. This option requires collaterals of 100% of the amount. Collaterals shall be in the form of guarantees provided by credit institutions or mutual guarantee societies.

Proposals may be rejected when:

- It is not considered credible by the Spanish Public Authorities that consortium members could adequately co-finance the project.
- Project deadlines are not considered realistic by the Spanish Public Authorities
- Accredited Technical or financial capacities of Spanish consortium members are not considered realistic to fulfil the project as submitted.
- Spanish partners do not provide enough proof of their capabilities.
- The effect or positive impact on selection and evaluation criteria is considered insufficient by the relevant authorities.
- Not enough relevance of Spanish consortium share.

Eligibility of the costs and funding

1. **Consortium configuration**

To be eligible, there is no minimum Spanish participation. However Spanish relevance should be detailed and will be assessed by MTDFP: projects considered not relevant for Spain may be rejected.
Participants shall set up a national sub-consortium with the following rules:

1) All members shall prove knowledge and expertise, and relevant contributions to the project in their relative project matters.

2) There shall be at least one SME in the Spanish consortium.

3) Each national sub-consortium will send its own form C

4) Each participant shall comply with the stated conditions to be a beneficiary at the moment national grant is awarded.

2. Solvency and Financial Conditions

- **MTDFP** will check if the participants are eligible monitoring that they are not in crisis as defined by EU regulation 651/2014.

- Each Spanish private partner has the necessary financial capacity to carry out the project, and the Spanish Public Authorities will assess it. **MTDFP** shall perform a financial analysis.

- **MTDFP** requires collateral equivalent to 100% of the national funding amount.

3. Funding rates

The funding rates provided by MTDFP will be defined in accordance with Regulation (EU) No 651/2014 (GBER) and the Framework for State Aid for Research, Development and Innovation (OJ 2014/C198/01), depending on the type of beneficiary and the project activity (RIA or IA). Funding rates will be defined for each call in due course.

For example, the funding rate provided by MTDFP for the Chips JU-ECS R&I calls will be set out as a percentage of the eligible costs, as shown in the following table:

Type of Beneficiary / Type of activity	Large Enterprise / RTO	Medium Enterprise / RTO	Small Enterprise / RTO
RIA (EPS) Research and Innovation Action	Up to 65% - JU%	Up to 75% - JU%	Up to 80% - JU%
IA (EPS) Innovation Action	Up to 40% - JU%	Up to 50% - JU%	Up to 60% - JU%

These percentages are maxima according to the funding provided by the Chips JU and the conditions stated by annex I and articles 25 and 28 of Regulation (EU) No 651/2014 related to definition of enterprise categories and maximum aid intensity.

MTDFP will never provide more than the Chips JU funding, and will never surpass the aforementioned limits in any case.

4. **Amount of required collateral by MTDFP**

MTDFP requires collateral of 100% of the national funding amount.

5. **Additional Information to be provided at submission and other conditions**

MTDFP will specifically encourage projects:

- Coordinated by a Spanish entity.
- Where there are SMEs working in the core of the project.
- Contributing to the territorial cohesion in semiconductor sector and industry, according to the III axis of the Spanish Recovery, Transformation and Resilience Plan
- Promote the presence and participation of women in semiconductor sector and industry, according to the IV axis of the Spanish Recovery, Transformation and Resilience Plan
- Where Spanish entities that have never participated in previous ECSEL or KDT calls are integrated in order to broaden the range of participants in Chips JU.

AEI
Legal requirements for eligibility of a partner or a project and eligibility of the costs and funding

1. **Legal requirements for the eligibility of a partner or a project**

a) Type or nature of participants

The AEI is the national authority which funds non-profit public R&D organizations such as:

- Public Research Centres
- Public and Private Universities
- Other non-profit R&D organizations, in which R&I activities are defined as the main objective.

The AEI has not defined any limit to the number of Spanish participants per project in the Chips JU calls.

b) Legal, administrative and financial conditions

About the proposal and project

2025 Chips JU ECS R&I and Chips for Europe calls will be managed by the "Subdivisión de Programas Científico-Técnicos Transversales, Fortalecimiento y Excelencia".

Applicants requesting national funds from AEI shall comply with the following regulations on grants:

- General Subsidies Law (Ley 38/2003)
- Science Law (Ley 14/2011)
- AEI Statutes (Real Decreto 1067/2015)
- All other regulation that apply to national PCI calls (National PCI call)

The projects granted by the AEI must be aligned with the main objectives described in the latest State Plan for Scientific and Technical Research and Innovation (more information at: MICIU).

The instrument for funding the Spanish groups will be the call "Proyectos de Colaboración Internacional" (PCI). As a reference, applicants are advised to read the call PCI 2024-1.

Participation in this program means acceptance and compliance with all the conditions stated on this document.

Any publication or dissemination activity resulting from the granted projects must acknowledge AEI funding even after the end of the project, according to national PCI call (see article 12.2 in the call text of PCI2024-1 for reference).

Calls supported by AEI in 2025 are according to Work Programme 2023-2027 – Version 10.0

- ECS R&I Calls · Chips Ju
  HORIZON-JU-Chips-2025-IA

  HORIZON-JU-Chips-2025-IA FT1

  HORIZON-JU-Chips-2025-IA FT2

  HORIZON-JU-Chips-2025-IA-HIA

  HORIZON-JU-Chips-2025-RIA

- Chips For Europe · Chips Ju
  HORIZON-JU-Chips-2025-IA-EDA

HORIZON-Chips-2025-1-IA-LEAI

DIGITAL-JU-Chips-2025-SG-SSOI

DIGITAL-JU-Chips-2025-SG-LFA

Additional document. AEI Annex – "Declaración Responsable"

Applicants have to send to the AEI (to: era-ict@aei.gob.es cc: beatriz.gomez@aei.gob.es) the document "Declaración responsable" duly signed by the Spanish Principal Investigator. They must send it until one week after the deadline of the Project Outline (PO) stage of the call.

Bellow you can find the content of the document to be signed. It is available on the web site Convocatorias Internacionales | Agencia Estatal de Investigación for download.

c) Consortium configuration

Spanish Principal Investigators must demonstrate experience as investigators in projects funded by the Plan Estatal I+D+i 2013-2016, or subsequent plans or other relevant national or international programmes.

Incompatibility (read carefully)[35]**:**

- Principal Investigators can only apply for funding in only one proposal in 2025 ECS R&I Chips and Chips for Europe Calls funded by AEI, including RIA, IA and others. If one PI submits two or more proposals, he/she will be declared ineligible in all but one.
- Principal Investigators will not be eligible for funding in more than one proposal in a PCI call of the same year or consecutive years. This should be taken into account when participating in other ERA-NETS or international programmes funded through the PCI call.
- Principal Investigators must remain unchanged between the proposal in PO stage to this transnational call and the PCI call. Only force majeure reasons will be accepted to change a principal investigator (see point one of incompatibilities).
- To this end, and to avoid any issue, the Principal Investigator must be clearly identifiable in the Chips JU documents as main contact point, when possible, and always with "leading" in "Role of researcher (in the project)" field of the proposal template and must comply with these rules. Otherwise, he/she will be declared ineligible for funding by the AEI.

d) Other conditions

[35] See the below "Declaración responsable".

2. Eligibility of the costs and funding

a) Eligibility of costs

AEI will fund those tasks in the work packages indubitably related to research and technology development and innovation, not considering as such if only mere communication or dissemination or similar activities. Please contact AEI in advance to check eligibility.

AEI grants follow the rules of marginal costs, with a maximum request of 350.000 € (including direct + indirect costs) per participant or 50% of the total costs of the Spanish applicant part of the project (whichever amount is lower). In any case, the total grant (AEI + Chips JU) will be a maximum 100% of the total project costs.

Eligible costs are:

1. Personnel costs: Contracts (gross remuneration and contributions to social security) exclusively intended to the funded project implementation. Fellowships are not eligible.
2. Current costs, disposable materials, travelling expenses and other costs that can be justified as necessary to carry out the proposed activities.
3. Indirect costs (overheads), 25% of the direct eligible costs (see points 1 and 2).

If the Spanish participant is the Chips project coordinator, the maximum request can be up to 500.000€ (including direct + indirect costs) or 50% of the total costs of the Spanish part of the project (whichever amount is lower).

Centers formed by different Spanish legal entities will be considered as a unique entity, and thus the maximum funding should not exceed the limits per proposal established above (f.i. mixed centers).

Chips projects are granted by the Chips JU and AEI on the basis of a single budget per project, but with two complementary funding sources. This means that both the Chips JU and AEI finance the total project, not item by item. Double funding (overlapping with other EU or National funding) will be avoided and projects or parts of projects already funded will be not granted. Final funding will take into account the transnational evaluation of the collaborative proposal, the scientific quality of the Spanish group, the benefit of the international collaboration, the participation of the industrial sector, and the resources available.

Every institution funded by the AEI should justify the total costs of the project regardless of the origin of grants (Chips JU or AEI). Therefore, every institution funded by the AEI must submit a valid audit certificate with the total costs of the project.

*b) National public funding rates (**N/A**)*

Type of action/Type of Beneficiary	**Large enterprise**	**SME**	**Public Research Institutes and Universities**
Research and Innovation action			
Innovation Action			

"Declaración responsable" to be sent to AEI (to: beatriz.gomez@aei.gob.es**)**

Available on the web site Convocatorias Internacionales | Agencia Estatal de Investigación for download.

NOTA IMPORTANTE
La presente declaración responsable se atendrá a lo establecido en el artículo 69 de la Ley 39/2015, de 1 de octubre, del Procedimiento Administrativo Común de las Administraciones Públicas.

Según el citado precepto, la inexactitud, falsedad u omisión, de carácter esencial, de cualquier dato o información que se incorpore a una declaración responsable o a una comunicación, o la no presentación de la documentación que sea en su caso requerida para acreditar el cumplimiento de lo declarado, determinará la imposibilidad de continuar con el procedimiento dando lugar a la desestimación de la ayuda o en su caso su revocación, sin perjuicio de las responsabilidades penales, civiles o administrativas a que hubiera lugar.

Asimismo, se recuerda que tal y como establece el artículo 58.a) de la Ley 38/2003, de 17 de noviembre, General de Subvenciones, se considerará falta muy grave la obtención de una subvención falseando las condiciones requeridas para su concesión u ocultando las que la hubiesen impedido o limitado.

DECLARACIÓN REPONSABLE

D/Dña.……,
NIF.:……, con domicilio en……
……..……..……, teléfonos de contacto: ……..…… en nombre propio y como investigador(a)

principal español(a) de la propuesta con título ……..…….…….…….…. y acrónimo ……..…. de la convocatoria …..…… del año …… en la que participa la Agencia Estatal de Investigación (AEI) como agencia financiadora española.

DECLARO RESPONSABLEMENTE EN NOMBRE PROPIO Y COMO INVESTIGADOR(A) PRINCIPAL DE LA PROPUESTA QUE:

1. Estoy en posesión del grado de doctor/a, o
2. Pertenezco a un centro contemplado en el *Directorio de centros tecnológicos y centros de apoyo a la innovación tecnológica regulados por el Real Decreto 2093/20228*, estoy en posesión de la titulación universitaria de licenciado/a, ingeniero/a, arquitecto/a o graduado/a, y, además, cumplo con una de las siguientes condiciones:
    a. Tengo acreditada experiencia en actividades de I+D+i durante al menos cinco años.
    b. He dirigido proyectos de investigación en el marco de las convocatorias de proyectos de I+D+i del plan estatal de I+D+i 2013-2016 o posteriores
3. Cuento con autorización expresa de la entidad beneficiaria para participar en la solicitud de la propuesta ……(ACRONIMO).
4. No estoy contratado/a con cargo a los fondos obtenidos en ninguna convocatoria de los planes estatales de I+D+i actual o anteriores, *con excepción* de las correspondientes al Programa Estatal de Promoción del Talento y su Empleabilidad en I+D+i o equivalentes en las que se requiera estar en posesión del grado de doctor/a, o de las ayudas «Severo Ochoa» y «María de Maeztu» de la AEI.
5. Tengo una relación funcionarial, estatutaria, laboral u otro vínculo profesional con la entidad beneficiaria de la ayuda o con otra entidad que cumpla los requisitos de elegibilidad de las ayudas durante toda la duración de la acción[36], o
6. En el caso de que el vínculo profesional con la entidad beneficiaria sea menor a la duración de la acción, aporto una declaración de la entidad beneficiaria comprometiéndose a mantener la vinculación durante toda la duración de la acción.
7. En el caso de que mi vinculación laboral no sea con la entidad beneficiaria sino con otra, cuento con la autorización expresa de ésta para participar en la solicitud presentada por la entidad beneficiaria.
8. Cuento con experiencia (no necesariamente como investigador principal) en proyectos financiados por alguno de los Planes Estatales desde 2013, en proyectos del Programa Marco Europeo de I+i, incluidas las ayudas del Consejo Europeo de Investigación u

[36] La expectativa de nombramiento o contratación con motivo de haber superado un procedimiento de selección de personal en concurrencia competitiva convocado por cualquier entidad del sector público, según la definición del artículo 2 de la Ley 40/2015, de 1 de octubre, se considerará vinculación suficiente

otros programas nacionales o internacionales relevantes tal y como muestran las referencias de proyectos concedidos en los que he participado que se incluyen en el anexo[37].

9. No soy beneficiario de un ayuda de Proyectos de Colaboración Internacional del año 2025[38].
10. Solo presento una propuesta a la presente convocatoria[39].
11. No he presentado otra propuesta (incluso que no haya sido evaluada) en convocatorias transnacionales (proyectos bilaterales, ERA-NET, partenariados europeos o *partnerships*, u otros programas internacionales como CRCNS de la *National Science Foundation* estadounidense, los grupos de interés EIG-Concert-Japan y EU-CELAC, entre otros), que puedan ser financiadas por las convocatorias de "Proyectos de Colaboración Internacional" de 2025 o 2026 de la AEI.
12. No he presentado otra propuesta a la convocatoria de "Proyectos de Generación de Conocimiento 2024. **Proyectos tipo I (PID-I)"[40].**

Anexos:

- Anexo 1. Lista de proyectos más relevantes financiados por los planes nacionales o/y estatales, así como de los programas marco de investigación e innovación de la Unión Europea u otros relevantes en los que he participado.
- Anexo 2. Declaración de la entidad beneficiaria comprometiéndose a mantener la vinculación del investigador principal durante toda la duración del proyecto. *Solo para los investigadores principales que tengan una vinculación con la entidad beneficiaria menor a la duración del proyecto.*

En ……..…… a …….. de ……..…….…… de ……...

Fdo.: (Nombre completo y dos apellidos).

[37] En caso de no tener experiencia en proyectos de los planes estatales y nacionales mencionadas, puede informar de proyectos en los que haya participado para su valoración.
[38] No es compatible tener dos ayudas Proyectos de Colaboración Internacional del mismo año o de dos años consecutivos: 2024-2025, 2025-2026, 2026-2027.
[39] Si un mismo investigador principal presenta dos o más propuestas a la presente convocatoria, todas podrán ser declaradas no elegibles, sin posibilidad de cambio de IP.
[40] Los otros tipos de proyectos de PID (no encuadrados en I) no tienen ninguna incompatibilidad con PCI.

Sweden

National contact persons for Chips JU

Country	Name	First name	Tel	E-mail
Sweden	Saavedra Granholm	Adela	+46 8 473 31 50	adela.saavedragranholm@vinnova.se
Sweden	Gustafsson	Lars	+46 8 473 32 12	lars.gustafsson@vinnova.se
Sweden	Brundin	Sverker	+46 8 473 31 97	sverker.brundin@vinnova.se

Detailed information for Swedish applicants in Chips JU is available at:

Chips Joint Undertaking – Vinnova

Legal requirements for the eligibility of a partner or a project

Type or nature of participants

Calls are open for public and private companies of all sizes as well as for universities and research institutes in Sweden.

Funding conditions

The costs of all partners specified in the project budget and in the reporting to Vinnova shall harmonize with costs in accordance with the Grant Agreement with Chips JU and the costs reported to Chips JU, respectively.

Only legal entities are eligible for funding, natural persons will not be funded.

Consortium configuration

The total eligible project costs of participating Swedish companies must amount to at least 60% of the aggregated eligible project costs of all Swedish participants in the project consortium.

Legal, administrative and financial conditions

Participating companies must have fulfilled fiscal obligations and must be able to cover their own expenses for the duration of the project.

- Participating companies must be registered as a limited company in Sweden (Aktiebolag).
- Participating companies must have a permanent establishment in Sweden.
- Project activities must be conducted at sites that belong to a participating company. Project costs must belong to the participating company.
- Participating companies must be registered for employer's contribution.
- Participating companies must have submitted at least two annual reports to the Swedish Companies Registration Office (Bolagsverket).
- The company's most recent annual report/ financial statement should show that net sales or equity correspond to at least 50% of the public funding applied for from Vinnova and Chips JU.

Swedish SMEs must also show when submitting the full project proposal (FPP) that they:

- Have an annual net turnover of at least 1 million SEK according to the latest annual report.
- Have a minimum of three full time employees.

Net turnover does not include public funding from, for example, Vinnova or the EU Commission.

To calculate how big a company is, the EU's definition of small and medium-sized companies is applied: Användarhandledning om definitionen av SMF-företag (vinnova.se)

Other conditions

Vinnova helps to build Sweden's innovation capacity, contributing to sustainable growth. We make it possible for organisations to address challenges together by enabling innovation that makes a difference. All projects that Vinnova funds within Chips JU are expected to contribute to this mission.

Vinnova will check if the Swedish applicants are eligible considering the national eligibility rules, including Vinnova's terms and conditions for grants. In addition to that, Vinnova will assess the national relevance of the international project proposal based on the information about the Swedish applicant's contribution to the project, Vinnova's projects portfolio and national priorities.

Swedish applicants to Chips JU Calls 2025 **must** submit a joint National Part with the international full project proposal (FPP). In case the applicants fail to submit the National Part with the international FPP, they will be considered **not eligible for national funding**. In the National Part, participating companies are required to provide a credible description

of the project's impact on the company's technological knowledge, economic growth and future assets in Sweden. Participating universities or research institutes are required to provide a credible description of the project's impact on the university's or research institute's scientific and technological knowledge base and positive impact on Swedish society in general. It is important that each partner clearly describes their role in the project, their goals with the project, how they will benefit from the project and added value from international collaboration. The Swedish consortium needs to specify in the National Part to which goals of Agenda 2030 the project contributes to and how the Swedish consortium contributes to the integration of gender equality aspects in the project.

A template for the Swedish National Part is available at Vinnova's website for the Chips JU Calls 2025.

If the international project proposal is selected for funding in Chips JU Calls 2025, the Swedish consortium must submit one joint national application to Vinnova. The project description attached to the national application should be based on the National Part submitted together with FPP application to Chips JU. After PAB decision on projects selected for funding in Chips JU Calls 2025, Vinnova will contact the Swedish applicants to provide a template for the national application för funding and specific information about the submission process.

Vinnova obtains information about the credit status of all applicant companies prior to the national funding decision. The applicants must comply with the national rules and special conditions for participation in Chips JU

on the date of the national decision.

Vinnova uses information we receive from credit reports, currently from Dun & Bradstreet.

For us to grant funding, the following applies:

- Organizations seeking funding for personnel costs must be registered as employers with the Swedish Tax Agency (Skatteverket).
- Organizations must not be insolvent or undergoing liquidation or corporate restructuring. They must also not have unpaid debts with the Swedish Enforcement Authority (Kronofogdemyndigheten).
- Limited liability companies must not have used up half or more of their share capital.
- If requested, SMEs must be able to demonstrate that they have the financial means

to carry out the project according to their budget in the application. They cannot use public grants or own funds intended for other projects to cover project costs in this call.

Eligible costs and funding rates

Vinnova's terms and conditions

§ 6.1 (Eligible costs) in Vinnova´s terms and conditions for funding is replaced by the eligible costs and the calculation of these specified in the Grant Agreement with Chips JU. Otherwise Vinnova's general terms and conditions for national funding applies. In addition, observe Vinnova's national rules and special conditions for participation in Chips JU applies. For further details, please see the full version of the national eligibility rules in the Vinnova website for the Chips JU Calls 2025.

Funding rates

In the table below the national funding rates for Swedish participants in Chips JU are presented. The funding rates must be within the limits given by State Aid Rules. Vinnova grants funding in accordance with Article 25 of the EU Commission's General Block Exemption Regulation (GBER). In this call, we provide companies with support for industrial research.

In this the call for proposals Vinnova also provides support to organisations that do not engage in economic activities. This means that they do not offer a service or product on a market. This usually includes universities, research institutes and other organisations. The maximum funding rate is 65% for participating universities and research institutes in Chips JU Calls 2025.

Please be aware that EU contribution doesn't count as state aid.

	Large Enterprises	Small and Medium Enterprises	Universities and Research Institutes
RIA - Research and Innovation Action	25%	35%	50%
IA - Innovation Action	20%	30%	50%
Focus Topics	20%	30%	50%

Project Coordinator	Large Enterprises	Universities and Research Institutes
RIA - Research and Innovation Action	40%	65%
IA - Innovation Action	35%	65%
Focus Topics	35%	65%

Additional information and other conditions

- Maximum Vinnova contribution to one project is limited to 2 000 000 €
- The maximum funding from Vinnova for a single large enterprise, university and research institute is equivalent to 730 000 €.
- The maximum funding from Vinnova for a small and medium enterprise is equivalent to 450 000 €.
- Vinnova use the exchange rate for Euro/SEK of the ECB on the date of Chips JU call FPP phase deadline.

Switzerland

National contact person for Chips JU programme

Country	Name	First	Phone	email
Switzerland	**Euresearch (NCP)**			
	Llewellynn	Timothy	+41 31 380 60 18	timothy.llewellynn@euresearch.ch
	Fighera	Marianna	+41 31 380 60 24	marianna.fighera@euresearch.ch
	SERI (national cofunding)			
	Rusconi	Giudy	+41 58 463 27 95	giudy.rusconi@sbfi.admin.ch

Contact Euresearch with general questions regarding Swiss participation in the Chips JU calls.

The State Secretariat for Education, Research and Innovation (SERI) is providing national cofunding. Information on the Chips JU national cofunding is found here and here.

1. Legal requirements for the eligibility of a partner or a project

a) Type or nature of participants

All Swiss entities are eligible to request funding for their research and innovation activities in Switzerland related to a Chips JU project.

b) Consortium configuration

No national requirements on consortium configuration.

c) Other conditions

The research and innovation activities for which funding is requested need to take place in Switzerland.

2. Eligibility of the costs and funding

d) National public funding rates

Listed below are the maximum national funding rates per action type. The total available Budget for 2025 will be evenly distributed across successful Swiss participants.

Type of action/Type of Beneficiary	**Large enterprises**	**SME**	**Public Research Institutes and Universities**
Research and Innovation Action	up to 10%	up to 35%	up to 35%
Innovation Action	up to 10%	up to 30%	up to 35%

Türkiye

National contact person for Chips JU programme

Country	Name	First	Phone	email
Türkiye	GEZİCİ KOÇ	Özlem	+903122981772	ncpdis@tubitak.gov.tr
Türkiye	TİFTİK	Hasan Burak	+903122981752	ncpdis@tubitak.gov.tr

TUBITAK, www.tubitak.gov.tr

The National Funding Authority (NFA) of Türkiye for Chips JU is the Scientific and Technological Research Council of Türkiye (TUBITAK). Principal legal regulations and documents on the public funding of research, development and innovation in Türkiye are available on the TUBITAK websites.

1. Legal requirements for the eligibility of a partner or a project

a) Type or nature of participants

Calls are open for public institutions and private companies of all sizes as well as for universities and research institutes in Türkiye.

b) Legal, administrative and financial conditions

Eligible participants can be funded via TUBITAK 1071 Programme. The national rules and the procedure for application will be available on TUBITAK website.

c) Consortium configuration

There is no limitation for the consortium configuration.

d) Other conditions

Only legal entities are eligible for funding. Natural persons will not be funded.

2. Eligibility of the costs and funding

e) Eligibility of costs

- Personnel cost
- Travel costs

- Expenditures for consumables
- Expenditures for instruments, equipment, software that would be used for R&D purposes
- Expenditures for subcontracting and other services need for R&D work

f) National public funding rates

Type of action/Type of Beneficiary	**Large enterprise**	**SME**	**Public Research Institutes and Universities**
Research and Innovation action	%60-EU Contribution	%75-EU Contribution	%100-EU Contribution
Innovation Action	%60-EU Contribution	%75-EU Contribution	%100-EU Contribution

g) Additional Information to be provided at submission and other conditions.

- The total Turkish funding budget for Chips 2025 NI Call (including Initiative call IA-EDA is TBD) is 6 000 000 €.
- There is no pre-allocated distribution of the Turkish funding budget between the NI Calls in 2025, nor to specific topics of any of the NI Calls in 2025.
- While determining the project budget in national applications, the international project budget and the exchange selling rate of the Central Bank of the Republic of Turkey on the date of national application are taken as basis.
- Participants are subject to TUBITAK 1071 Programme rules.

United Kingdom

National contact person for the Chips JU programme

Country	Name	First Name	Tel	Email
United Kingdom	Sharp	Craig	+44 7920 750631	craig.sharp@iuk.ukri.org
	Morris	Ben	+44 7795 641229	ben.morris@iuk.ukri.org

National Funding Agency: Innovate UK

Innovate UK provides funding to support and stimulate innovation in the UK economy and the wider international CR&D&I ecosystem. We do this by encouraging businesses to work with other commercial and research organisations. We largely require that projects are led by businesses. Other types of organisations can apply in collaboration with a business partner.

It is important to note that a successful application to Chips JU does not guarantee funding by Innovate UK. UK participants are strongly advised to discuss applications with their Innovate UK contacts prior to submission to Chips JU.

1) **Legal requirements for the eligibility of a partner or project Type or nature of participants**

The UK will support UK participants, as listed, in projects selected by the Chips Joint Undertaking Non- Initiative.

- registered business of any size
- academic institution
- public sector organisation
- research and technology organisation (RTO)

Only legal entities will be funded, natural persons will not be funded.

2) **Legal, administrative and financial conditions Consortium configuration**

- must contain at least one UK registered business of any size
- can collaborate with other UK registered organisations

More information on the different types of organisation can be found in our Funding rules. Academic institutions cannot lead or work alone.

Innovate UK will assess the financial viability (liquidity) and eligibility of UK applicants. As this is a joint undertaking, then those entities who fail the Undertakings in Difficulty test will be deemed ineligible for funding. EUR-Lex - 02014R0651-20210801 - EN - EUR-Lex (europa.eu)

3) Other conditions

UK applicants to Chips JU Calls 2025 must submit a joint National Part with the international full project proposal (FPP). In this National Part, participating UK companies must provide a credible description of the project's impact on the company's technological knowledge, capability, economic growth and benefits to the UK. Participating universities or research organisations must provide a credible description of the project's impact on the university's or research organisation's scientific and technological knowledge and benefit for the UK. It is important that each UK partner clearly describes their role and goals with the project, how they will benefit from it and the added value from this international collaboration.

On successful evaluation and receipt of the project approval, from the Chips JU, Innovate UK will send successful applicants documentation to complete for national processes. On successful evaluation and receipt of the project approval, from the Chips JU, Innovate UK will send successful applicants documentation to complete for national processes.

4) Eligibility of the costs and funding

a) Eligibility of costs

The eligibility of costs is in accordance with Innovate UK national rules on eligible costs. For details on the eligibility of costs see the national Cost Guidelines can be found here on the Innovate UK Costs Guidance webpage.

UK funded work must be carried out in the UK and your project costs must be incurred in the UK.

b) Funding and funding rates

Innovate UK has a budget of up to £10,000,000 for UK participation in the Chips JU 2025 Horizon Europe call(s) (ECS and Chips for Europe Initiative)

UK applicants can apply for a total UK co-funding grant of up to £750,000 in a single proposal (note this does not preclude a request for a higher amount), if your total UK co-funding grant is greater than £750,000, then you must provide justification by email to support@iuk.ukri.org as soon as possible before you start your application and at least 10 working days before the competition closes, where we will decide whether to approve your request.

Subcontracting is limited to 20% of total UK eligible costs.

In the event that the UK receives more successfully approved projects from Chips JU, then Innovate UK reserves the right to take a portfolio approach.

Co-Funding from Innovate UK will equal the following in Chips JU Horizon Europe funded ECS calls below:

Action	Topic	Large	Medium	Small	RTO/Uni
HORIZON-JU-Chips-2025-IA	**Global call according to SRIA 2024 (IA)**	**50%-JU%**	**60%-JU%**	**70%-JU%**	**100%-JU%**
HORIZON-JU-Chips-2025-IA-HIA	**Heterogeneous integration for high-performance automotive computing**	**50%-JU%**	**60%-JU%**	**70%-JU%**	**100%-JU%**
HORIZON-JU-Chips-2025-IA FT1	**RISC-V Automotive Hardware Platform**	**50%-JU%**	**60%-JU%**	**70%-JU%**	**100%-JU%**
HORIZON-JU-Chips-2025-IA FT2	**AI-assisted Methods and Tools for Engineering Automation**	**50%-JU%**	**60%-JU%**	**70%-JU%**	**100%-JU%**
HORIZON-Chips 2024-2-RIA-T1	**Global RIA**	**50%-JU%**	**60%-JU%**	**70%-JU%**	**100%-JU%**

UK research organisations undertaking non-economic activity as part of the project can share up to 30% of the total UK eligible project costs. If your consortium contains more than one UK research organisation undertaking non-economic activity, this maximum is shared between them. Of that 30% you could get funding for your eligible project costs of up to:

- 80% of full economic costs (FEC) if you are a Je-S registered institution such as an academic
- 100% of your project costs if you are an RTO, not for profit organisation, public sector organisation or research organisation.

For Chips for Europe Initiative calls (Appendix 6) please get in touch with the UK National Contacts.