APPENDIX 6: ACTIVITIES LAUNCHED IN 2025 FOR THE CHIPS FOR EUROPE INITIATIVE PART

Version 2

CONTENTS

1 ACTIVITIES 2025 CHIPS FOR EUROPE INITIATIVE PART

This appendix foresees the launch of the following call topics with an estimated EU expenditure of as below:

HE ACTIONS		
Call Activities		
Topic	**Description**	**Indicative EU budget M€**
HORIZON-JU-Chips-2025-RIA-SUP	Support for start-ups and SMEs	**220**
HORIZON-JU-Chips-2025-CSA	Pan-European infrastructure for Chips Design Innovation	**12**
HORIZON-JU-Chips-2025-IA-EDA	Open-source EDA tools development	**20**
HORIZON-JU-Chips-2025-FPA-QAC3	Establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilot Lines	**0**
Lab to Fab	Lab to Fab accelerator European ecosystem for chiplet integration	**50**
Other Activities		
HORIZON-JU-Chips-2025-SGA-QAC1	Supporting developing Quantum Chip Technology for stability Pilot Lines	**50**
HORIZON-JU-Chips-2025-SGA-QAC2	Supporting developing Quantum Chip Technology for high-quality Trapped Ions Pilot Line	**20**
DEP ACTIONS		
Call Activities		
Topic	**Description**	**Indicative EU budget M€**
Call for tenders	Cloud platform for the European Design Platform	**15**
DIGITAL-JU-Chips-2025-CSA-DET	Set-up and integration of Design Enablement Teams	**5**
DIGITAL-JU-Chips-2025-SG-SSOI	Accelerator for Advanced Strained Silicon on Insulator Substrates	**30**
DIGITAL-Chips-2025-1-IA-LEAI	Low-power Edge AI Chips	**20**
TOTAL		**442**

The board recognizes the need for a Lab-to-Fab action to strengthen the contacts between companies and other users to the Chips JU funded pilot lines that are presently being set up and foresees, provisionally, a specific call on this topic in the work programme with a budget of 50 million Euro.

2 TECHNICAL DESCRIPTION OF THE CALL TOPICS

2.1 Design Platform

Semiconductor circuit design involves the development of integrated circuits (ICs) and system-on-chips (SoCs) by defining the functionalities and specifications of chips, capturing a significant share of the value within the semiconductor supply chain. The industry is increasingly shifting towards more complex, application-specific, and highly integrated semiconductors, making state-of-the-art design essential for competitiveness and differentiation across various applications. In this evolving landscape, fabless companies are uniquely positioned to lead technological innovation and address the demands of diverse applications, further solidifying their critical role and driving growth within the semiconductor sector.

The Chips Act underscores the strategic importance of fostering chip design growth in Europe to enhance the competitiveness of the Union's semiconductor industry. Pillar I of the Chips Act, the Chips for Europe Initiative, outlines an ambitious plan to strengthen the Union's resilience in semiconductor technologies, including promoting the growth of fabless companies focused on leading-edge technologies. This is especially pertinent given that the European share of global fabless semiconductor companies' revenues has shrunk to critically low levels, highlighting the urgent need for strategic initiatives to bolster this sector and enhance Europe's competitiveness. A critical mass of fabless companies is also key to generate further demand that would justify increased investment in semiconductor manufacturing capacity in Europe.

Recognising the Union's limited fabless capacity, and the significant barriers to entry in chip design, the Design Platform focuses on nurturing emerging companies in the sector. The Design Platform is at the heart of the Chips for Europe Initiative and is envisaged as a key instrument to foster the development of a strong design ecosystem in the Union by creating a pipeline of highly innovative European fabless companies, focusing particularly on the growth of start-ups and SMEs.

In 2024, the Chips Joint Undertaking launched a call for the selection of a Platform Coordination Team (PCT). The selected PCT shall assist the Chips JU in defining the technical specifications of a cloud service for the platform to be procured by the Chips JU through a dedicated Call for Tenders. This cloud infrastructure shall incorporate all the services necessary for the efficient implementation of the Design Platform including repositories, a user authentication service, license usage monitoring and any relevant *Infrastructure as Code* to be deployed at the various Design Enablement Teams (DETs).

The PCT will be complemented by a number of DETs that shall set up a cloud-based environment for users designing on the platform, support them in their design cycle, and facilitate access of users to foundry services. Furthermore, the DETs shall be responsible for

providing access to foundry services. In fact, it shall be a pre-requisite that for an entity to become a DET, it must act as, or be linked to, a foundry aggregator.[1]

These DETs may be design houses and RTOs with the necessary expertise and experience in providing such services. They can be spread geographically but may also have different sectoral (e.g. defence) or technological (e.g. digital, analogue, photonics) focus. The selection of DETs shall take place via an open and inclusive process, based on fulfilment of certain technical and security requirements. Any design service provider fulfilling such requirements may apply for integration into the platform. The PCT shall provide the set of requirements that DETs must fulfil in order to apply for integration in the cloud-based platform.
To this end this work programme includes the following topics:

- Cloud platform for the European Design Platform
- Design Enablement Teams
- Support to start-ups and SMEs.
- Open-source EDA tools development
- Low power Edge AI Chips

[1] A foundry aggregator is an industry standard term used for companies that act as an intermediary between fabless semiconductor companies (clients) and semiconductor foundries (manufacturers). Typically, only large enterprises directly engage with foundries.

2.1.1 Cloud platform for the European Design Platform

Type of Action	Call for tenders
Indicative EU budget (from the DEP budget)	15 M€
Mode	EU funding only

2.1.1.1 Context

Note: A formal call for tenders shall be published over the course of 2025. The current text shall not be considered as a formal Call for Tenders within the context of a procurement procedure. Information listed here is purely indicative.

Chip design is a key weakness in Europe's semiconductor ecosystem. Fabless revenues in Europe represent less than 1% of global revenues. Recognising the importance of this sector to the value chain, Pillar 1 of the Chips Act, the Chips for Europe Initiative foresees a design platform to enable start-ups and SMEs to venture in design. The Design Platform is foreseen to serve as a hub of services and resources for its users and to this end the Chips Joint Undertaking shall procure a cloud infrastructure to enable the implementation of said platform. The cloud infrastructure shall include both the underlying cloud service as well as any related development of custom software.

2.1.1.2 Scope

The central cloud infrastructure shall host the IP, PDKs and open-source EDA tools as well as training services. This shall be accompanied by a user authentication service. Interested parties shall therefore be responsible for the provisioning and management of a secure and scalable cloud infrastructure capable of hosting these key elements of the Design Platform and its associated services. The selected service provider shall be responsible for the setting up and maintenance of this service for 4 years.

This shall be accompanied by a vendor-neutral software solution for automated infrastructure configuration, referred to here as Infrastructure as Code (IaC), to be deployed at the various Design Enablement Teams as part of a federated cloud infrastructure for the Design Platform. The purpose of this IaC shall be to:

- **Standardise deployment**: The IaC should enable the Platform Coordination Team (PCT) to define and enforce a standardised configuration for DET cloud environments through code, ensuring that all DETs adhere to the same security protocols, service level agreements, and access controls. This would ensure a more consistent and reliable user experience across different DETs.
- **Automate provisioning**: The IaC related tools should be used to automate the provisioning of cloud resources for DETs. This would simplify the process of setting

up and scaling design environments, reducing the potential for manual errors and freeing up DET resources to focus on user support and other value-added services.

- **Ensure version control and reproducibility**: Through the IaC, the PCT should be able to leverage version control systems to track changes and ensure that environments can be easily reproduced. This shall be crucial for maintaining consistency over time, simplifying troubleshooting, and facilitating the rollback of changes if needed.
- **Enhance security and compliance**: The IaC can help enforce security best practices by automating security configurations and checks. This could be particularly relevant for the DP, given the sensitive nature of design data and IP. By codifying security policies, the PCT could help ensure a more secure and compliant design environment for all users.

2.1.1.3 Expected outcomes.

The requested cloud services shall primarily contain the following elements:

- A repository populated with an extensive portfolio of open-source and proprietary 'design assets' to facilitate and enhance the design process for users, such as intellectual property (IP) blocks, design templates, fast adoption kits, process design kits (PDKs) from pilot lines and open foundries, open-source design tools, as well as reusable open-access design elements from previous EU-funded projects.

- Any suitable features, such as user authentication and license usage monitoring, that are deemed useful for the management of the overall initiative and the various DETs in the Design Platform.

- Templates of virtual machines or containers containing all the software components and configuration required to operate a given electronic design software, and that can be easily deployed on the cloud instances operated by the DETs.

The selected tender shall also be responsible for the running and maintenance of this service for 4 years.

The latter point shall be complemented by the development of an *Infrastructure as Code* (IaC) framework that supports a variety of cloud vendors. Work related to the development and management of the IaC shall be coordinated by the PCT and deployed across various DETs. The purpose of this IaC is to facilitate cloud deployment at the various DETs, ensure baseline security standards, and provide a consistent experience across different DETs. Where possible, cloud vendor-agnostic resources shall be used, accompanied by vendor-specific configurations where necessary. The service of developing the IaC shall also be procured by the Chips JU with the technical assistance of the PCT.

All resources involved in this development shall be based in the EU, including the location of the cloud-related data centres.

Further details will be presented in the Call for Tenders when published.

2.1.2 Set-up and integration of Design Enablement Teams

Topic: DIGITAL-JU-Chips-2025-CSA-DET*

Type of Action	CSA
Indicative EU budget	5 M€
Expected EU contribution per project	The JU estimates that an EU contribution of around EUR 0.5 million would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	EU funding only One stage Call with submission of Full Proposal (FPP)
Call launch date	TBD
Deadline FPP Phase	TBD

***DISCLAIMER**: **The details of the call (including their timing) will be adjusted following negotiations with the Platform Coordination Team that was selected based on the calls DIGITAL-Chips-2024-CfEoI-CDP-1 and DIGITAL-Chips-2024-CSA-CDP-1**

2.1.2.1 Context

Semiconductor circuit design is the process of creating integrated circuits (ICs) and system-on-chips (SoCs) by defining the functionalities and characteristics of chips, capturing a substantial portion of the added value within the semiconductor value chain. The trend is moving towards more complex, application-specific, highly integrated semiconductors, making cutting-edge design crucial for competitiveness and differentiation in a wide range of applications. In this context, fabless companies are well-positioned to drive technological advancements and meet the needs of diverse applications, reinforcing their pivotal role and growth in the semiconductor industry.

The Chips Act underscores the strategic importance of fostering chip design growth in Europe to enhance the competitiveness of the Union’s semiconductor industry. Pillar I of the Chips Act, the Chips for Europe Initiative, outlines an ambitious plan to strengthen the Union's resilience in semiconductor technologies, including promoting the growth of fabless companies focused on leading-edge technologies. This is especially pertinent given that the European share of global fabless semiconductor companies’ revenues has shrunk to critically low levels

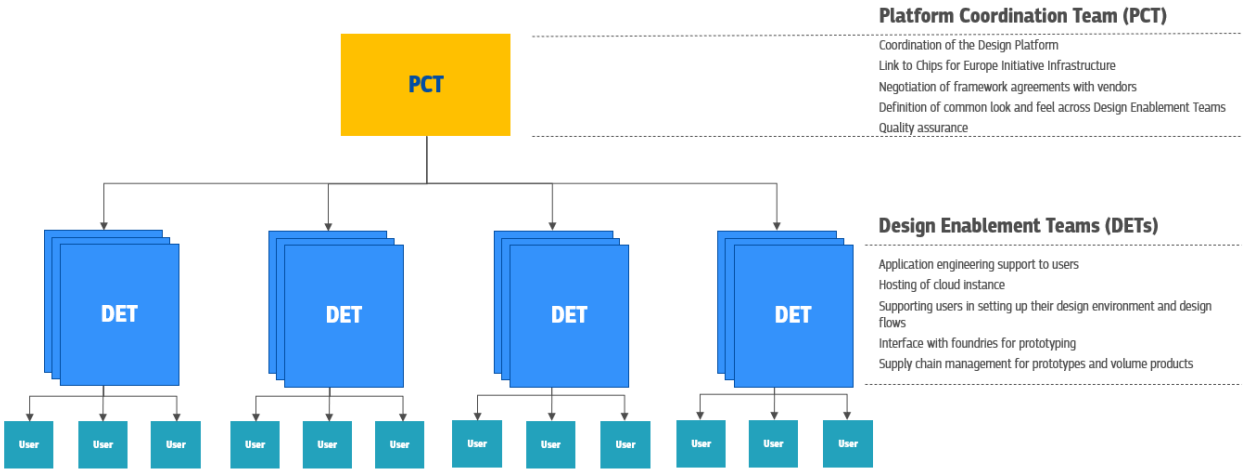
(currently around 1%), highlighting the urgent need for strategic initiatives to bolster this sector and enhance Europe's competitiveness. A critical mass of fabless companies is also key to generate further demand that would justify increased investment in semiconductor manufacturing capacity in Europe.

Recognising the Union's limited fabless capacity, and the significant barriers to entry in chip design, the Design Platform shall focus on nurturing emerging companies in the sector. The Design Platform is at the heart of the Chips for Europe Initiative, it is envisaged as a key instrument to foster the development of a strong design ecosystem in the Union, by creating a pipeline of highly innovative European fabless companies, focusing particularly on the growth of start-ups and SMEs.

At the core of the design process lie a series of Electronic Design Automation (EDA) tools, Intellectual Property (IP) blocks and Process Design Kits (PDKs) including standard cell libraries. This is coupled with either on-premises or cloud-based computing resources. Each of these elements requires a separate acquisition process for the designer, often involving very significant costs and its own complex procedures.

2.1.2.2 Scope

The Design Platform shall act as a hub of services to support European companies engaged in chip design. Besides providing digital resources, the platform shall include services to facilitate, optimise and accelerate the design process for start-ups and SMEs. To this end, Design Enablement Teams (DETs) shall play a crucial role in supporting and accompanying users in their chip development process until tape-out.



Responsibilities in the Design Platform should be shared along the lines of the central and distributed services. These two elements of the overall architecture can be distributed to two main classes of implementing partners:

- **Platform Coordination Team (PCT)** in charge of the central cloud service, framework agreements with EDA/IP suppliers and coordination of the initiative. A key condition for members of the PCT consortium is neutrality, for this reason it is foreseen that the consortium is potentially composed of not-for-profit organisations, such as Research and Technology Organisations (RTOs) and other neutral entities. Through internal expertise and, where necessary, sub-contracting, these entities shall design and implement the overarching technical implementation of the platform and design interfaces with the distributed services.
- **Design Enablement Teams (DETs)** each of which is in charge of managing a distributed cloud instance, dedicated application engineering support to users from setting up their design environment and design flows up to tape out. DETs can be selected among providers of chips design support services, such as design houses, RTOs or other entities interested in providing design enablement services. DETs shall be designated in terms of their technology expertise (e.g., digital, analogue, mixed-signal, etc.), ability to offer support across the end-to-end design flow, access to fabrication services and a proven track record of delivering high quality services to users, amongst other characteristics.

The scope of this topic is to designate a number of Design Enablement Teams. This follows a call for Design Platform to select a Platform Coordination Team that was launched in July 2024.

2.1.2.3 Expected outcomes.

The core functions of DETs include, but are not limited to:

1. **Running Electronic Design Automation (EDA) tools on the cloud**: DETs will manage cloud instances from a cloud provider of their choosing, facilitating access to essential design tools and simulation environments.
2. **Design flow support and customisation**: they will assist users in setting up and customising design environments and flows, ensuring smooth progression from initial setup to tape-out.
3. **Application engineering**: DETs will offer dedicated application engineering support, addressing specific user needs and challenges throughout the development process.
4. **Access to Process Design Kits (PDKs)**: users will be provided with access to the necessary PDKs for their design projects.
5. **Prototyping and fabrication services**: DETs will facilitate prototyping and fabrication services through partnerships with leading foundries or aggregators, and the Chips for Europe Initiative pilot lines or other relevant pilot lines.

Each DET shall manage a cloud instance from a cloud provider of its choosing, and offer dedicated application engineering support to users, from setting up their design environment

and design flows to tape-out. The level of security of that cloud instance shall be commensurate to the expected categories of users and applications that are expected to be running on this instance.

It is anticipated that initially a limited set of DETs will be required to cover an adequate set of tools and technologies necessary to support most startups. DETs can be ASIC design houses, RTOs, or other entities interested in providing design enablement services. DETs will be designated based on their technology expertise (e.g. digital, analogue, mixed-signal, etc.), ability to offer support across the end-to-end design flow, including PPA optimisation, access to fabrication services, and a proven track record of delivering high-quality services to users, among other characteristics.

These DETs shall be public or private organisations that offer custom design support services, such as ASIC design houses and RTOs, with the necessary expertise and experience in providing such services. DETs should possibly have established relationships with foundries or alternatively have strong collaboration with aggregators enabling efficient communication with foundries. Overall, the DETs shall cover a wide variety of semiconductor technologies and can have different sectoral focuses (e.g. automotive, defence).

The only eligible costs for each beneficiary selected as DET through the call evaluation are those directly related to the integration of DET's cloud services into the design platform. This integration will be executed through the deployment of an Infrastructure as Code solution developed specifically for the design platform to ensure a consistent user experience. The PCT will provide this solution to each selected DET. Any costs related to the development of services and integration of EDA tools over the infrastructure of the cloud provider of choice, are considered to be part of the standard business proposition and competitive offering of the DET; as such, these costs are not considered eligible.

The DETs will be selected in order to ensure support to as many available technologies as possible.

2.1.2.4 Admissibility

Admissibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Regarding page limits:

- The page limit for the chapter RELEVANCE is 20 pages.
- The page limit for the chapter IMPLEMENTATION + chapter 4 of the template for the proposal (Part B) is 60 pages.
- The page limit for the chapter IMPACT is 20 pages.

2.1.2.5 Eligibility

Eligibility conditions are described in Annex 2 of the WP General Annexes.
The following exceptions apply:
Subject to participation restrictions for the protection of European digital infrastructures, communication and information systems, and related supply chains, as described in Annex 4 of the WP General Annexes.
Legal entities that are established in the Union or EEA countries but are controlled from third countries may only participate on the condition that they guarantee the protection of the essential security interests of the Union and the Member States and that they ensure the protection of classified documents information. Where applicable, security guarantees need to be provided after proposal selection.

2.1.2.6 Financial and operational capacity and exclusion

Please refer to Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

2.1.2.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).
For the priority order of proposals with the same score, please refer to Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

2.1.2.8 Award criteria.

Please refer to Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Specific rules may apply regarding the eligibility to national funding.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.1.2.9 Scores

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)

Relevance	0-5	1	3
Implementation	0-5	1	3
Impact	0-5	1	3
Total	0-15		10

(*) threshold applies to unweighted score.
(**) the weight is only used to establish the ranking of the proposals.

2.1.2.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to DIGITAL.

Type of beneficiary	**Maximum EU Contribution as % of eligible costs according to DIGITAL**
For profit organization but not an SME	100%
SME (for profit SME)	100 %
University/Other (not for profit)	100 %

2.1.3 Support for start-ups and SMEs

Topic: HORIZON-JU-Chips-2025-IA-SUP

The text in this subsection should be seen as a placeholder. The exact manner in which the funding will be allocated will be defined in a later stage.

Support to start-ups and SMEs making use of the Design Platform

Specific conditions	
Type of Action	To be decided
Indicative EU budget	EUR 220 million.
Mode	To be decided.

2.1.3.1 Context

A key goal of the Design Platform is to overcome a critical barrier in the growth of EU fabless companies: access to funding, foundries, design tools, computing resources and IP.

Fabless startups are key drivers of innovation, playing a crucial role in advancing technologies such as AI chips, telecommunications, and advanced automotive systems. These companies are at the forefront of technological breakthroughs, driving progress in critical sectors. Despite their contributions to 50% of global integrated circuit (IC) revenues, Europe currently captures less than 1% of this market. This underscores a significant opportunity for growth in the global semiconductor industry.

Investing in fabless startups offers high returns on investment with limited capital requirements. The design process, which accounts for a significant share of the value of final products, is far less capital-intensive than manufacturing, making it an affordable yet lucrative opportunity. Moreover, these startups are renowned for their efficiency, agility, and rapid scalability, with multiple exit strategy options, including acquisitions or stock market listings. Aligning with EU strategic priorities, fabless start-ups can currently look towards initiatives such as the Chips Fund, the STEP programme, competence centres, and pilot lines, amplifying their potential for success and impact. However, there is a crucial gap at the very early stages for these companies which the Design Platform can address through a dedicated support programme.

Beneficiaries may provide financial support to third parties. The support to third parties can only be provided in the form of grants. Financial support provided by the participants to third parties is one of the primary activities of the action to be able to achieve its objectives. Given its level of ambition, the maximum amount to be granted to each third party is EUR 8 million.

2.1.3.2 Scope

In addition to the general activities of the Design Platform that are open to all eligible users in Europe in line with any applicable access conditions, additional activities can be subject to other limitations. The selected Platform Coordination Team (PCT) will be in charge of running a start-up/SME incubation and accelerator programme in collaboration with the selected Design Enablement Teams (DETs). As part of a suite of support services provided to selected start-ups participating in the incubation and accelerator programmes, a grant covering certain pre-determined eligible costs will be provided.

Grants to third parties as part of the accelerator programme need to be commensurately matched by Participating States of the Chips Joint Undertaking.

This programme will facilitate the scaling up of start-ups engaged in chip design through favourable conditions. The PCT will undertake the selection of these start-ups under the guidance of the Chips Joint Undertaking.

2.1.3.3 Expected outcomes.

A main element in the Design Platform is a **start-up and SME incubation and acceleration programme** that is broadly based on two levels of support and a funnel-like architecture as seen in Figure 1.

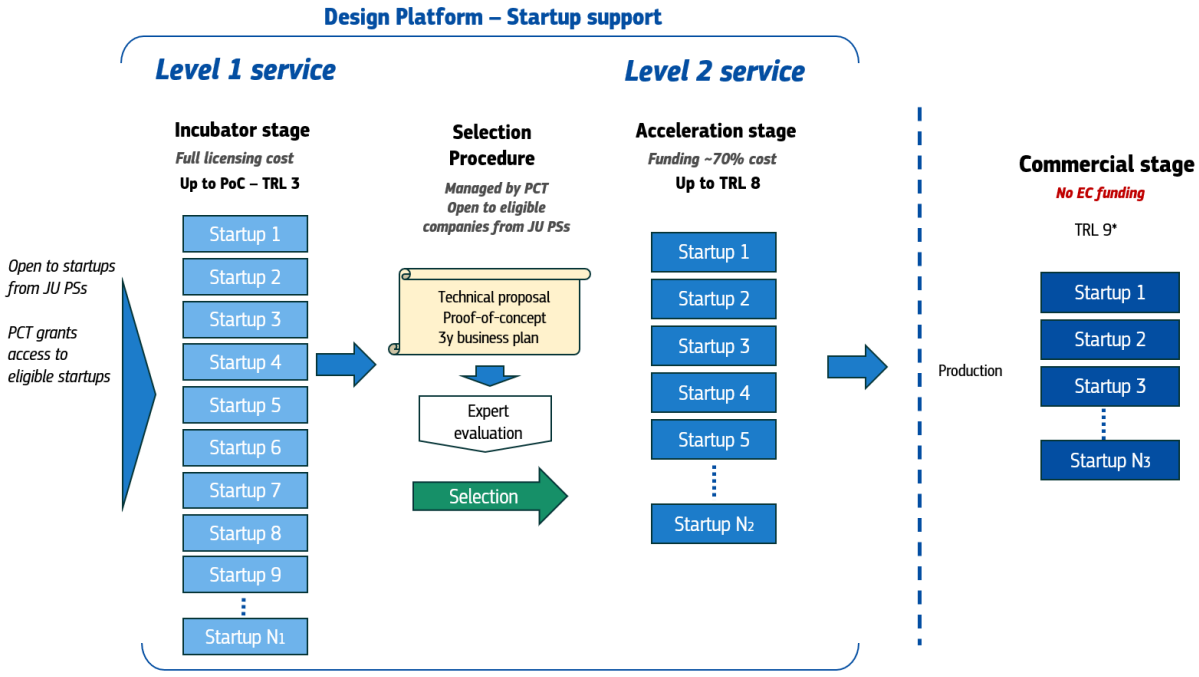


Figure 1 - Design Platform start-up support programme

Level 1 support will be as broadly open to European start-ups and SMEs as possible. Here users will be given access to *proof-of-concept* licenses that are usually subject to nominal fees. These fees will be financed by the Union through a third-party support from the selected consortium,

without contributions from the Chips JU's Participating States. Level 1 support is primarily aimed at spinouts with limited funding.

Promising start-ups and SMEs at a more advanced stage of development may proceed through an additional selection process to qualify for the Level 2 programme, which offers funding to cover up to 70% of the costs for the selected companies. Eligible costs for Level 2 grants include EDA licenses, IP licenses, DET support, cloud computing, and foundry costs such as masks and tape-out. EDA license costs will be determined by the Master Framework Agreement negotiated by the Platform Coordination Team of the Design Platform.

Start-ups and SMEs in Level 2 can expect two main funding streams – an EU budget component and a Participating State component. Selection shall be subject to the approval of the Public Authorities Board of the Chips Joint Undertaking.

Concretely, the following outcomes are expected:

- A swift albeit rigorous selection procedure for both Level 1 and Level 2 services, with multiple cut-off dates throughout the year. Selection must consider both the technical merits of a project as well as the business case and market viability of the eventual product.
- A pool of experts that evaluate the proposals, those experts will be professionals from the field (semiconductor manufacturing) with at least 15 years of experience in a business environment, understanding both the technology and the business, markets. Payment of the experts will be based on market conditions.
- A system of coordination with Participating States of the Chips Joint Undertaking on issues related to co-funding.
- A system of coordination and collaboration with the office of the Chips Joint Undertaking on the selection of start-ups and SMEs.
- Participation of 100 fabless start-ups and SMEs in the accelerator programme by 2028.

2.1.4 Open-source EDA tools development

Topic: HORIZON-JU-Chips-2025-IA-EDA

Type of Action	Innovation Action (IA)
Indicative EU budget	20 M€
Expected EU contribution per project	The Chips JU estimates that an EU contribution of between EUR 6 and 7 million per project would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Two stage Call, with submission of Project Outline (PO) and Full Project Proposal (FPP)
Call launch date	04 March 2025
Deadline PO	29 Apr 2025 at 17:00 Brussels Time
Deadline FPP Phase	17 Sep 2025 at 17:00 Brussels Time

2.1.4.1 Context

A key objective of the Chips Act under the Chips for Europe Initiative is the 'building up of advanced design capacity for integrated semiconductor technologies'. To this end as part of operational objective 1 of the Chips Act, the Initiative shall integrate 'new design facilities with extended libraries and electronic design automation (EDA) tools' into a virtual design platform. As part of a broader suite of resources, the Design Platform will make available a number of open-source tools.

Chip design is a vital element in the semiconductor value chain and open-source Electronic Design Automation (EDA) tools can be key drivers for innovation in this sector by enabling researchers and developers to experiment with new algorithms, architectures, and methodologies.

Access to EDA software, essential for chip development, has traditionally been both heavily restricted and prohibitively expensive, creating significant barriers for start-ups and small-to-medium-sized enterprises (SMEs). Open-source EDA tools can empower start-ups and SMEs with cost-efficient alternatives to expensive commercial licenses, allowing SMEs to

experiment with chip design. This is particularly crucial for SMEs operating in low- to mid-volume production.

Moreover, Europe is facing a considerable workforce shortage in this sector. This requires the cultivation of an open ecosystem to attract and develop more designers and developers. Open-source EDA tools lower the barrier of entry to chip design and thus attract new engineers and chip designers. Students and new entrants in the field can experiment with chip design without limitations on exploitation of their design or restrictive non-disclosure agreements (NDAs), fostering learning and experimentation. Therefore, wide-spread dissemination of these tools can help in addressing the skills gap in the semiconductor industry.

Existing open-source toolchains already support complete chip designs in several mature nodes, which are the technology of choice in a number of applications in fields such as radar design, automotive, aeronautics and space, medical technology, and electronics for harsh environments—industries with a strong European market presence. With relatively low tape-out costs, these nodes present minimal barriers for SMEs, and open-source tools could enable a wide array of European companies and start-ups to enter the chip design arena.

The growing accessibility of low-cost computing resources has opened the door for large-scale exploitation of parallel computing in EDA. However, this potential is often constrained by licensing costs, which limit the number of parallel runs needed for comprehensive adoption. This is an area where open-source implementations can be an interesting proposition. The ability to fully leverage computational resources for unrestricted parallel scaling—especially with the integration of modern machine learning technologies—has become a focal point of interest for many organisations seeking to push the boundaries of innovation.

Therefore, it is expected that over time, open-source EDA tools will offer significant benefits across other areas of chip design, including advanced nodes and highly integrated digital circuits, fostering growth and enhancing efficiency across the entire electronics sector.

The Horizon Europe *Go-IT* project[2] and the FOSSI Foundation have developed a roadmap for open-source hardware. This roadmap should be considered in proposals answering to this call.[3]

Proposals should, where relevant, build upon existing open-source resources and focus on advancing these tools to the next level. Efforts should include bridging the gap between open-source and commercial EDA tools - proposals should include a realistic outline with expectations and objectives to achieve this goal. Overall, proposals should include effective strategies for enhancing existing tools and improve user experience while driving innovation by introducing novel tools and methodologies. Where appropriate, machine learning techniques to improve performance and productivity should be considered.

Technology Readiness Level: Targeted TRL at the end of projects is between 7 and 8.

2 Go IT! | GOIT | Project | Fact sheet | HORIZON | CORDIS | European Commission
3 Roadmap and Recommendations for Open Source EDA in Europe

2.1.4.2 Scope

Each proposal must address only one of the following three streams: (i) digital SoC design; (ii) analogue and mixed-signal design; or (iii) productivity, interoperability, and verification. Only one project per stream will be selected.

(i) Digital SoC design

Modern integrated circuit (IC) design thrives on digital workflows and advanced design automation tools, enabling engineers to capitalise on the increasing circuit density achieved with each new technology node. The exponential progress driven by Moore's Law not only fuels innovation at the industry's forefront but also broadens accessibility across the technological landscape, including at more mature nodes. While much attention is given to cutting-edge design nodes, the enhanced productivity these advancements bring also empowers SMEs, even those with limited design expertise, to undertake projects previously beyond their reach. This democratisation of IC design opens up new markets, fosters innovation, and drives growth across the sector.

Digital chip design serves as the backbone for developing processors, memory, and logic components that power a vast array of electronic devices—from smartphones and computers to IoT systems and cutting-edge AI hardware. Currently, open-source EDA tools for digital design provide sufficient support for mature technology nodes. However, advancing to more sophisticated nodes requires refining existing tools and expanding their functionality. As technology nodes become smaller, the impact of parasitic effects on overall performance—both in terms of power and timing—grows significantly. Continued development is essential to accurately model and mitigate these effects.

(ii) Analogue and mixed-signal design

For stable, mature nodes, the availability of open-source Process Design Kits (PDKs) and comprehensive open-source design flows already provides significant opportunities for analogue and mixed-signal integrated circuit (IC) design. These tools are particularly valuable for education and training, enabling students, researchers, and engineers to gain hands-on experience in designing, manufacturing, and testing custom analogue and mixed-signal chips. By lowering the cost and accessibility barriers, these resources play a crucial role in equipping the next generation of designers with practical skills, particularly in fields such as sensors, communication systems, and signal processing.

Looking to the short-to-medium term, the goal is to achieve performance and reliability on par with proprietary tools while expanding the capabilities of open-source EDA solutions. Specific focus will be given to advancing tools and methodologies for complex analogue, radio frequency (RF), and terahertz (THz) designs, as these are essential for emerging technologies such as IoT, 5G/6G, and advanced communication systems. By prioritising analogue and mixed-signal functionality from the outset, open-source EDA tools can drive innovation and expand access for this key segment of Europe's semiconductor ecosystem.

(iii) Productivity, interoperability, and verification

Addressing the challenge of labour shortages requires targeted measures to enhance efficiency and accessibility in chip design. In the short term, further developing and leveraging open-source tools can significantly boost productivity by reducing barriers to entry for engineers and designers.

In the short-to-medium term, focusing on improving interoperability between various Electronic Design Automation (EDA) tools will be crucial. Seamlessly integrating open-source EDA tools into established design workflows will enable smoother collaboration between diverse teams and disciplines. This interoperability will reduce time-consuming inefficiencies caused by incompatible systems, streamlining the design process from conceptualisation to final tape-out. For SMEs, in particular, this integration will lower technical barriers, making advanced chip design more accessible and cost-effective.

Furthermore, investing in open-source design verification tools will deliver benefits to the entire chip design industry. Fast and efficient verification solutions with minimal access barriers are essential for accelerating time-to-market and fostering wider adoption. In the medium term, the development of innovative verification methodologies will further enhance efficiency, streamline design processes, and attract skilled talent from diverse disciplines, addressing the industry's growing demand for expertise.

Such advancements will not only address immediate labour shortages but also strengthen the productivity of European SMEs in key industries, supporting their innovation in a rapidly evolving global market.

2.1.4.3 Expected outcomes.

Results stemming from this call should be well documented and widely disseminated. Precise documentation, user manuals as well as video tutorials should be made available. Selected consortia must develop teaching materials and courses with open resources and examples based on the developed/improved open-source EDA tools, accessible to academic institutions across the EU and suitable for self-study by individuals. To this end, collaboration with initiatives such as EUROPRACTICE is encouraged.

Consortia should actively engage with the Platform Coordination Team of the Chips Act's Design Platform to integrate their tools into the platform's design flows. Proposals must outline a clear strategy for engaging with relevant foundries to secure access to the required PDKs.

Proposals should clearly specify the applicable OSI-approved open-source license for all results. Proposals should also include a sustainability plan for results following the end of the project.[4]

The three selected consortia should collaborate in their technical work where relevant. Joint communication and dissemination efforts are encouraged.

The expected outcomes for each of the aforementioned streams are the following:

4 https://opensource.org/licenses

(i) Digital SoC design

The overall ambition of this stream is to ensure a comprehensive and stable digital design flow in more mainstream nodes (65-28nm). Improvement of tools in more mature nodes is also within scope of this stream. To this end a baseline for the quality of results currently achievable with current state-of-the-art open-source tools needs to be determined.

The following outcomes shall be considered:

- **Improved open-source EDA tools**: Achieved better result quality and performance of existing open-source EDA tools, especially for large-scale designs.
- **Optimised parasitic extraction workflow**: Delivered enhanced accuracy and efficiency in parasitic extraction, validated through experimental results on fabricated integrated circuits (ICs).
- **Industry-standard memory generators**: Developed high-quality memory generators for both mature and advanced technology nodes, meeting industry requirements.
- **Enhanced hierarchical design flows**: Strengthened support for hierarchical design methodologies and incremental build processes.
- **Timing and power analysis:** Robust tools for timing and power analysis for more advanced technology nodes.
- **Efficient SoC integration frameworks**: Provided streamlined frameworks for system-on-chip (SoC) integration, incorporating comprehensive verification support and design-for-test capabilities.
- **Open synthetic benchmark set:** Developed a publicly available synthetic benchmark set specifically designed for the evaluation and calibration of open EDA tools, facilitating improved performance analysis and comparison.
- **Open solutions for die-to-die communication**: Delivered open technological solutions for direct die-to-die communication, conforming to industry standards and incorporating the development of associated application development kits (ADKs).
- **Advanced tools for system-in-package design**: Developed cutting-edge tools to support system-in-package (SiP) designs.
- **Standardised interfaces for design tool interoperability**: Collaborated across streams to standardise interfaces between analogue, mixed-signal, and digital design tools, improving interoperability and simplifying design workflows.
- **Prototyped tapeouts for open-source tool validation**: Demonstrated tapeouts for mainstream and advanced nodes designed with open-source tools, enabling calibration and guiding mid- to long-term priorities.
- **Enhanced formal equivalence checking**: Improved the coverage and reliability of formal equivalence checking for critical elements of the design flow.

(ii) Analogue and mixed-signal design

The overall ambition of this stream is the development of a full analogue/mixed-signal design flow. The emphasis should extend beyond improving existing tools to include the adoption of innovative approaches and new paradigms.

The following outcomes shall be considered:

- **High-performance analogue and mixed-signal simulators**: Delivered advanced analogue and mixed-signal simulation tools with efficient RF simulation capabilities, incorporating techniques such as shooting Newton analysis, harmonic balance analysis, transient noise simulation, and large-signal noise simulation.
- **Advanced electromagnetic simulation tools**: Developed state-of-the-art tools for electromagnetic (EM) simulations to support complex design needs.
- **Enhanced layout tools for parasitic extraction**: Achieved fast and accurate parasitic netlist extraction from large circuit layouts, incorporating netlist reduction techniques to improve efficiency.
- **Efficient custom layout generation tools**: Provided tools for efficient custom layout generation, combining programmatic approaches with AI-assisted manual layout capabilities.
- **Standardised interfaces for tool interoperability**: Collaborated across streams to standardise interfaces between analogue, mixed-signal, and digital design tools, ensuring improved interoperability and seamless workflow integration.
- **Robust EM simulation capabilities**: Delivered comprehensive EM simulation solutions with efficient data exchange between design entry tools and circuit simulators.
- **Curated tool collections and Integrated Design Environments**: Maintained and supported curated tool collections and integrated design environments, reducing barriers to entry and enabling standardised frameworks for IP generation.
- **Open-source IP generation frameworks**: Facilitated the creation of IP under open-source licence terms, including detailed documentation, verification test benches, and silicon validation results.

(iii) Productivity, interoperability, and verification

The overarching aim of this stream is to enhance productivity by adopting innovative design approaches and ensuring seamless data exchange between tools. This will be complemented by the development of robust verification processes that accommodate diverse methodologies and effectively tackle the increasing complexity of modern chip design.

The following outcomes shall be considered:

- **High-speed mixed-mode simulation tools**: Delivered advanced simulation capabilities supporting both HDL or gate-level designs and analogue components for efficient mixed-mode analysis.
- **Tailored verification environments**: Enhanced verification tools and methodologies, creating robust environments specifically designed for analogue and mixed-signal designs.
- **Improved waveform viewing tools**: Developed enhanced waveform viewing tools with features such as automated waveform analysis, backtracing functionalities, and improved usability.
- **Standardised tool interfaces for interoperability**: Collaborated across streams to standardise interfaces between analogue, mixed-signal, and digital design tools, improving interoperability and streamlining design workflows.
- **Curated tool collections for IP generation**: Maintained and supported curated tool collections and integrated design environments, reducing barriers to entry and enabling standardised processes for IP creation and management.

- **Modular frameworks for design and verification**: Developed modular frameworks enabling custom integration of design and verification transformations.
- **Open data exchange guidelines**: Established requirements and guidelines for open data exchange formats to facilitate seamless communication between tools and systems.
- **Usability improvements for open-source EDA tools**: Implemented general usability and accessibility improvements to existing open-source EDA tools, meeting the needs of a diverse user base.
- **Support for industry-standard verification**: Provided robust support for industry-standard verification methodologies, integrating them with innovative verification technologies.
- **Cross-domain verification capabilities**: Enabled effective cross-domain verification across various abstraction levels, including hardware/software co-design.

2.1.4.4 Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.
Regarding page limits:

Chapter	PO Phase	FPP Phase
Excellence	60 pages	60 pages
Impact	60 pages	100 pages
Quality and efficiency of the Implementation	60 pages	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

2.1.4.5 Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions:

Size limit	30 Participants
Max EU Contribution per partner (% of the total EU funding)	40%

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes).

Participation is limited to legal entities established in EU Member States, Norway, Iceland, Associated Countries, OECD and Mercosur countries (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled by a non-eligible country or by a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees provided by their eligible country of establishment, that their participation to the action would not negatively impact the Union's strategic assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

2.1.4.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

2.1.4.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

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2.1.4.8 Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.1.4.9 Score

The scores will be given with a resolution of one decimal. The score table is for PO and FPP.

Criteria	Range	Weight (**)	Threshold (*)
Excellence	0-5	1.0	3
Impact	0-5	1.5	3
Quality and efficiency of the implementation	0-5	0.7	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

2.1.4.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	Maximum EU Contribution as % of the Eligible Cost according to HE (*)
For profit organization but not an SME	20 %
SME (for profit SME)	30 %
University/Other (not for profit)	50 %

(*) beneficiaries may ask for a lower contribution.

2.1.5 A Pan-European infrastructure for Chips Design Innovation

Topic: HORIZON-JU-Chips-2025-CSA

Type of Action	Coordination and Support Actions (CSA)
Indicative EU budget	12 M€
Mode	EU funding only One stage Call, with submission of Full Project Proposal (FPP)
Call launch date	04 March 2025
Deadline FPP	29 Apr 2025 at 17:00 Brussels Time

2.1.5.1 Context

This call relates to the second general objective of the Chips JU: "build up large-scale design capacities for integrated semiconductor technologies"; and the seventh objective: "foster a dynamic Union-wide ecosystem based on digital value chains with simplified access to newcomers", including the active involvement of Academia, RTOs, and SMEs. This call aims at supporting the follow-up, extension and consolidation of EUROPRACTICE services to provide Europe with an open-access platform to design and fabricate chips.

2.1.5.2 Expected Outcomes

Proposals are expected to address the following expected outcomes:

Here are the outcomes with the title capitalisation removed in the bold parts:

- **Establish a platform for the European design ecosystem**: Created a platform that supports the growth of a European design ecosystem by fostering design reuse, enabling the exploitation of advanced technologies in various application domains, and providing a foundation for deep-tech startups.
- **Encourage dissemination of PDKs through the platform**: Actively supported foundries in sharing open-source and proprietary technologies, particularly their PDKs, via the platform.
- **Streamline access to EDA tools**: Simplified and lowered barriers to access commercial and open-source industry-standard EDA tools across various technologies, with a focus on affordability.

- **Enhance workforce skills through hands-on experience**: Reduced barriers for undergraduate and postgraduate students to gain hands-on IC design experience, complementing their theoretical coursework.
- **Provide diverse chip design flows**: Offered a variety of chip design flows, supporting multi-vendor configurations where feasible, and assisted users in customising their design workflows.
- **Facilitate affordable prototyping access**: Enabled academia, research centres, and spinouts to prototype affordably using industrial-grade and emerging technologies, including advanced nodes, mature nodes, open-source solutions, and pilot-line technologies, with pathways to volume production.
- **Offer extensive training resources**: Delivered comprehensive training resources to up-skill and re-skill students and professionals across a wide range of technologies.
- **Train academics and instructors through 'train-the-trainer' programmes**: Provided targeted training for educators in semiconductor and photonics technologies to improve teaching quality and dissemination.
- **Provide a platform for open-source IP exchange**: Established a platform for sharing open-source IP, fostering collaboration and reuse.
- **Support students in gaining hands-on chip design experience**: Facilitated pre-tertiary and vocational students' access to open-source tool flows, promoting practical engagement with chip design.
- **Ensure access to customer support and leading-edge tools**: Simplified access to customer support, IP, and cutting-edge design tools for a broad user base.
- **Lower barriers for advanced packaging and integration**: Supported users in adopting advanced packaging and heterogeneous integration techniques by reducing entry barriers.
- **Enable efficient fabrication and system integration**: Facilitated multi-project wafer (MPW) runs and small-volume fabrication of ASICs, photonics, MEMS, sensors, and their integration at the system level, while promoting the adoption of emerging or underutilised technologies such as quantum technologies, photonics, and wide-bandgap materials by academia and SMEs.
- **Promote technology offerings from research centres**: Supported and highlighted the technology services of research centres with lower TRL (technology readiness level) capabilities.

    - Furthermore, particular emphasis should be placed on ensuring the seamless integration of this initiative within the framework of the Chips Act. To this end, proposals must address the following outcomes:

- Collaborate extensively with initiatives under Pillar 1 of the Chips Act such as the Design Platform, competence centres and pilot lines. Particularly by:
    i. collaborating extensively with the Design Platform initiative, including through joint activities;
    ii. facilitating academic access to the Chips Act pilot lines;
    iii. support competence centres across all EU Member States.
- Implement a comprehensive plan to **integrate EUROPRACTICE services into the Chips Act's Design Platform before the conclusion of this project**.

2.1.5.3 Scope

Semiconductors are at the centre of strong geostrategic interests, and at the core of the global technological race. A priority for Europe is to strengthen its design capacity and to lower the barriers to get access to advanced semiconductor technologies. Amongst others, this requires the nurturing and supply of people with the right digital skills, and the provision of routes to prototype and commercialisation. Not only large enterprises, but also startups and academic institutions play a key role and are crucial in the European semiconductor value chain.

Proposals need to lower the entry-barrier for academia, research institutes and very importantly for startups, and SMEs by offering affordable access to a portfolio of industrial-grade design tools, IP blocks, including open-source ones (e.g. RISC-V based), and prototyping technologies. Services offered must include initial advice, training, support, reduced entry costs, prototyping and a clear route to chip manufacture and product supply. Proposals should include a KPI on start-ups and SMEs that use the services provided by the platform.

Furthermore, proposals should include some of the following elements:

- Fostering collaboration and support in Europe by providing a design IP exchange system, where members can exchange IP blocks, including commercialisation of academic designs, considering national rules if relevant.
- Supporting and stimulating the adoption of emerging technologies (e.g. neuromorphic, 3D integration, wafer-scale-packaging etc) by creating standardised platforms and make those widely accessible;
- Enabling heterogeneous system integration, such as the adoption of chiplets by a wide range of customers.
- Strengthening industry relevant skills by supporting up-skilling and re-skilling initiatives through provision of extended training activities.
- Integrating the initiative into the broader framework of the Chips Act.

Reminding that of general importance to the Chips JU calls are:

- Re-use of results from previous ECSEL/Chips JU, H2020 or EUREKA-cluster projects is encouraged.
- Developing synergies with other relevant European, national or regional initiatives and/or funding programmes.
- Encouraging SMEs to participate in those developments, in particular paying attention to the needs of SMEs, involve SMEs in project execution, and develop solutions that can be taken up and/or exploited by SMEs.

In this topic the integration of the gender dimension (sex and gender analysis) in research and innovation content is not a mandatory requirement.

2.1.5.4 Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Regarding page limits:

- The page limit for the chapter EXCELLENCE is 30 pages.
- The page limit for the chapter QUALITY AND EFFICIENCY OF THE IMPLEMENTATION is 30 pages.
- The page limit for the chapter IMPACT is 30 pages.

2.1.5.5 Eligibility

Applications will only be considered eligible if their content corresponds wholly (or at least in part) to the topic description for which they are submitted.

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Subject to restrictions for the protection of European communication networks (see Annex 1 of the WP General Annexes).

2.1.5.6 Financial and operational capacity and exclusion

Please refer to Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

2.1.5.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.1.5.8 Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.1.5.9 Score

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Excellence	0-5	1	3
Impact	0-5	1	3
Quality and efficiency of the implementation	0-5	1	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

2.1.5.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to Horizon Europe.

Type of beneficiary	EU Contribution as % of the Eligible Cost according to HE
For profit organization but not an SME	100 %
SME (for profit SME)	100 %
University/Other (not for profit)	100 %

2.1.6 Low power Edge AI Chips

Topic: DIGITAL-Chips-2025-1-IA-LEAI

Type of Action	Simple Grant
Indicative EU budget	20 M€
Expected EU contribution per project	The JU estimates that an EU contribution of between EUR 4 and 5 million would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Co-funded with the NFA One stage Call with submission of Full Proposal (FPP)
Call launch date	08 July 2025
Deadline FPP Phase	17 Sep 2025 at 17:00 Brussels Time

2.1.6.1 Expected Outcomes

Successful proposals are expected to deliver the following outcomes:

- Develop AI chip prototypes reaching TRL 6-7, integrating cutting-edge technologies such as non-volatile memories, neuromorphic computing, 3D heterogeneous integration, and photonic connectivity. These prototypes should be tested under real-world conditions and show potential for industrial scaling.
- Leverage the advanced capabilities of state-of-the-art infrastructures with fabrication and testing capabilities available within the Union, especially at leading Research and Technology Organisations (RTOs). This includes utilizing the Testing and Experimentation Facility (TEF) for Edge AI hardware (PREVAIL project[5]), a platform designed to accelerate the development of cutting-edge AI solutions, as well as Pilot Lines, including the ones of the Chips for Europe Initiative.
- The prototypes should demonstrate robust AI capabilities, including real-time inference, on-device learning, and adaptive decision-making. This enables edge AI systems to process data locally, make decisions, and adapt to changing environments without relying on cloud infrastructure, reducing latency and power consumption.
- The prototypes must achieve ultra-low power consumption to ensure energy-efficient AI operations in power-constrained edge environments, particularly for battery-powered devices. The emphasis should be on balancing computing power with energy efficiency.

5 https://prevail-project.eu/

- By advancing AI chips that are energy-efficient and highly secure, the developed technologies should contribute to Europe's digital transformation and help meet sustainability goals.

The ultimate goal of the project should be to drive the development of next-generation edge AI chips that combine high performance with ultra-low power consumption. These chips will enable real-time, on-chip AI capabilities for applications in fields like mobile communication networks (e.g. 6G), autonomous systems, industrial automation, and healthcare, all while aligning with Europe's sustainability and digitalization goals.

2.1.6.2 Scope

Proposals to this call should target the development of next-generation edge AI chips, specifically delivering high-performance, ultra-low-power AI hardware solutions for applications at the edge of the network. The main scope should be to develop, test, and prototype next-generation edge AI technologies leveraging the advanced capabilities of state-of-the-art infrastructure available in the Union, such as the Testing and Experimentation Facility (TEF) for Edge AI hardware (PREVAIL project) as well as Pilot Lines, including the ones of the Chips for Europe Initiative. The objective is to accelerate the transition of advanced ultra-low power edge computing technologies "from the lab to the fab", harnessing the facilities of leading European research and technology organizations.

The proposed edge AI chips shall be based on technologies that overcome the memory bottlenecks of classical "Von Neumann" computing architecture, enabling substantial performance gains, including:

- Solutions for computing in-memory, using Non-Volatile Embedded Memories, such as Magnetoresistive Random Access Memory (MRAM), Oxide-based RAM (OxRAM), and Ferroelectric RAM (FeRAM) technologies. critical for achieving energy-efficient AI processing by enabling fast, low-power data storage and retrieval.
- Unconventional architectures for neuromorphic and analogue computing, mimicking the brain's neural networks by employing alternative AI approaches such as spiking neural networks (SNNs) artificial neural networks based on magnetic tunnel junctions (MTJ)and specialized materials, thereby enabling real-time on-chip sensing, learning and inference with extremely low energy overhead, drastically reducing power consumption.
- Advanced 3D integration and packaging technologies for the efficient integration of heterogeneous components (such as memory, computing, and I/O) into a single compact chip. By using interposer technologies, die-to-wafer, wafer-to-wafer, and Through-Silicon Via (TSV) techniques, chip prototypes can reduce the overall system footprint, improving performance and energy efficiency.
- Photonic Integrated Circuits (PICs) for ultrafast, energy-efficient artificial neural networks, enhancing both computational efficiency and data transfer speeds with low

latency, ideal to ensure reliable high-speed connectivity in telecommunication networks and connected devices.

Proposals should target TRL 6-7 and demonstrate advancements in AI processing for real-time applications, while maintaining an emphasis on energy efficiency.

Consortia should be focussed on the realisation of the final prototype(s) and each partner should have a well-defined essential role towards the achievement of the objectives. Therefore, consortia are suggested to include strictly the participants that are required to cover the necessary tasks.

2.1.6.3 Admissibility

Admissibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Regarding page limits:

Chapter	PO Phase	FPP Phase
Relevance	60 pages	60 pages
Implementation	60 pages	100 pages
Impact	60 pages	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

2.1.6.4 Eligibility

Eligibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Specific eligibility conditions:

Size limit	70 Participants
Max EU Contribution per partner (% of the total EU funding)	50 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to participation restrictions for the protection of European digital infrastructures, communication and information systems, and related supply chains, as described in Annex 4 of the WP General Annexes.

2.1.6.5 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

2.1.6.6 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.1.6.7 Award criteria.

Please refer to Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes

Specific rules may apply regarding the eligibility to national funding.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.1.6.8 Scores

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Relevance	0-5	1.0	3
Impact	0-5	1.5	3
Implementation	0-5	0.7	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

2.1.6.9 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to DEP.

Type of beneficiary	**Maximum EU Contribution as % of the Eligible Cost according to DEP (*)**
For profit organization but not an SME	25 %
SME (for profit SME)	35 %
University/Other (not for profit)	35 %

(*) beneficiaries may ask for a lower contribution.

2.2 Accelerator for Advanced Strained Silicon on Insulator Substrates

Topic: DIGITAL-JU-Chips-2025-SG-SSOI

Type of Action	Simple Grant
Indicative EU budget	30 M€
Mode	Co-funded with the NFA One stage FPP
Call launch date	08 Jul 2025
Deadline FPP	17 Sep 2025 at 17:00 Brussels Time

2.2.1.1 Context

The continuous demand for higher-performing, energy-efficient semiconductor devices is driving the need for innovation in substrate engineering. Industries such as telecommunications, automotive, and consumer electronics require advanced solutions that can meet the growing complexity of applications like 5G/6G communications, autonomous driving, and edge AI/ML computing. As conventional silicon technologies approach their physical limits in terms of speed, power efficiency, and miniaturisation, Strained Silicon on Insulator (sSOI) substrates are emerging as a key enabler of the next generation of semiconductor devices. By introducing strain into the silicon layer, sSOI enhances electron mobility, offering significant performance gains in advanced nodes such as 7nm FD-SOI.

FD-SOI technology is already a vital asset for Europe, offering an excellent balance between power consumption, speed, and cost. However, as the technology scales down to the 7nm node, integrating sSOI substrates becomes essential to maintain these advantages. The unique properties of sSOI effectively address the challenges posed by smaller transistor sizes, enabling improved energy efficiency and sustained high performance. This makes sSOI a crucial component in meeting the demands of Europe's key markets, including mobile and infrastructure, automotive sensors, and IoT devices.

To bridge the gap between research breakthroughs and industrial-scale production, there is an urgent need for a dedicated accelerator that can handle the complexities of sSOI substrate development. Current R&D pilot lines lack the capacity and scale required to produce the thousands of wafers needed to ensure low defect densities and high manufacturing yields. An

accelerator is essential to enable this transition, ensuring that sSOI substrates can meet the rigorous requirements for integration into advanced FD-SOI manufacturing processes.

This accelerator will provide the necessary infrastructure to validate sSOI substrates on an industrial scale, accelerating their adoption within the European semiconductor ecosystem. By supporting high-volume production, manufacturers can assess the feasibility and cost-effectiveness of sSOI in large-scale FD-SOI applications. This initiative will reinforce Europe's leadership in semiconductor innovation, ensuring the industry remains competitive in the global market for advanced devices.

Moreover, the accelerator will foster collaboration across the semiconductor value chain—from material providers to foundries and system integrators. This cooperation will reduce the risks associated with new substrate technologies and promote the rapid commercialization of sSOI-based solutions. In doing so, it will contribute to Europe's strategic goals of technological sovereignty and sustainability in key high-performance sectors.

2.2.1.2 Scope

The proposed accelerator should address all levels of the key technological steps required to bring sSOI substrates to industrial scale:

- **Development of industrial-grade sSOI substrates** will focus on achieving low defect density, crucial for enhancing electron mobility and ensuring high-performance FD-SOI devices at the 7 nm node. This will involve refining **strain engineering techniques**, particularly to introduce a uniform global strain that can balance the performance for strained NMOS and relaxed PMOS transistors.
- Ensure compatibility with existing semiconductor manufacturing, the accelerator will refine **process integration and optimisation**. This includes improving epitaxial growth, wafer bonding, and defect reduction techniques to meet the requirements of advanced FD-SOI production processes.

Finally, the accelerator will **promote collaboration** across the semiconductor ecosystem, working with other pilot lines, as well as connecting to the design platform and competence centres, among others.

2.2.1.3 Expected Outcomes

The proposed accelerator shall be established with all the necessary equipment and facilities, and will target the following main **objectives**:

- Develop **industrial-grade sSOI substrates** with reduced defect density to improve **electron mobility** and overall device performance. These substrates should be capable of addressing the market entry of 7nm FD-SOI expected by 2030 as well as be fully compatible with existing FD-SOI technologies, including 22FDX and 18nm FD-SOI.
- **Develop scalable and cost-effective manufacturing processes,** ensuring compatibility with current industrial standards and promoting widespread adoption.
- Demonstrate the feasibility of integrating **strained NMOS and relaxed PMOS areas**, balancing the performance of both transistors.
- Accelerate the transition from R&D to industrial-scale production by providing a pre-industrial infrastructure capable of **producing several thousand wafers per year**.
- **Develop demonstrators** to validate the benefits of sSOI-based FD-SOI over competing FinFET technologies, particularly in terms of improved RF performance, lower noise, and reduced power consumption.
- Enable open access to Process Design Kits (PDKs) and design building blocks to foster the differentiation of FD-SOI technology, including stress and relaxation design elements.
- Enable early-stage design and system-level integration of sSOI substrates through Multi-Project Wafer (MPW) runs, allowing timely validation of substrate performance in real-world applications. Support design efforts for high-speed broadband RF circuits, mm-Wave radar systems, and compact low power automotive and IoT solutions as part of the Next Gen FD-SOI roadmap.

The **expected results** for this accelerator should therefore comprise:

- Create a **sustainable accelerator open to all European stakeholders**, providing access to state-of-the-art sSOI technology and manufacturing capabilities.
- **Develop and standardize Process Design Kits** based on validated sSOI substrate data, enabling designers to optimise their system-level architectures and meet the demands of next-generation applications. These PDKs should support the transition to 7nm FD-SOI technology, ensuring readiness for high-volume manufacturing by 2030.
- Expand the capabilities of sSOI substrates to **industrial-scale wafer production**, ensuring low defect densities and improved manufacturing yields that meet the rigorous standards of advanced semiconductor fabrication.
- Drive the creation of **intellectual property** and strengthen Europe's production capacity in sSOI technologies, contributing to Europe's leadership in critical semiconductor markets.
- With a particular focus on complementarity with the FD-SOI pilot line, foster collaborative development through **synergies with other Chips JU pilot lines**, enhancing the overall innovation capacity and technological leadership of Europe in semiconductor technologies,
- Provide comprehensive **training programs and skill development** initiatives to equip European technologists and engineers with the expertise necessary for sSOI substrate integration and advanced semiconductor manufacturing.

2.2.1.4 Admissibility

Admissibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Regarding page limits:

Chapter	FPP Phase
Relevance	60 pages
Implementation	100 pages
Impact	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

2.2.1.5 Eligibility

Eligibility conditions are described in Annex 2 "General DIGITAL EUROPE PROGRAMME conditions" of the WP General Annexes.

Specific eligibility conditions:

Size limit	70 Participants
Max EU Contribution per partner (% of the total EU funding)	50 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to participation restrictions for the protection of European digital infrastructures, communication and information systems, and related supply chains, as described in Annex 4 of the WP General Annexes.

Legal entities that are established in the Union or EEA countries but are controlled from third countries may only participate on the condition that they guarantee the protection of the essential security interests of the Union and the Member States and that they ensure the protection of classified documents information. Where applicable, security guarantees need to be provided after proposal selection.

2.2.1.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 2 “General DIGITAL EUROPE PROGRAMME conditions” of the WP General Annexes.

2.2.1.7 Evaluation procedure

For the specificity of each call evaluation please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.2.1.8 Award criteria.

Please refer to Annex 2 “General DIGITAL EUROPE PROGRAMME conditions” of the WP General Annexes

Specific rules may apply regarding the eligibility to national funding.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.2.1.9 Score

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Relevance	0-5	1.0	3
Impact	0-5	1.5	3
Implementation	0-5	0.7	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

2.2.1.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to DIGITAL.

Type of beneficiary	EU Contribution as % of the Eligible Cost according to DIGITAL (*)
For profit organization but not an SME	25 %
SME (for profit SME)	35 %
University/Other (not for profit)	35 %

(*) beneficiaries may ask for a lower contribution.

2.3 Quantum Chips

2.3.1 Establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilot Lines

Topic: HORIZON-JU-Chips-2025-FPA-QAC3

Type of Action	Framework Partnership Agreement (FPA)
Indicative EU budget	0 M€
Mode	One stage Call, with submission of Full Project Proposal (FPP)
Call launch date	TBD
Deadline FPP	TBD

2.3.1.1 Context

Europe's strategic agenda to lead in the field of quantum technologies by 2030 requires a concerted effort to develop advanced quantum chips including Quantum Processing Units (QPUs). This call seeks proposals for the development of new pilot lines capable of producing quantum chips, or the adaptation and expansion[6] of existing pilot lines in view of producing quantum chips.

The stability pilot lines should focus on achieving higher Technology Readiness Level (TRL) / Manufacturing Readiness Level (MRL) by advancing manufacturing and integration techniques tailored to meet the needs of the quantum industry over the next decade. The testing and experimentation facilities should be fully integrated in the pilot lines, providing seamless production and testing services.

Proposals are invited for pilot lines that address the production of any type of quantum chips for quantum sensing, quantum communication and quantum computing. Proposals should target the more mature quantum technologies like superconducting, photonic, semiconducting, diamond-based, or neutral atoms. Proposals should focus on robust, scalable quantum processing platforms that pave the way for the industrialization of the production of quantum chips and the commercialization of quantum chips. To achieve a diversified portfolio, no more than one pilot line per technology will be funded. Proposed platforms should build on quantum technologies complementing the approaches of the running Quantum Pilot Lines projects of the Chips for Europe Initiative.

Proposals are expected to indicate an overall budget for the implementation of a full FPA via multiple SGAs. In case of sufficient high-quality proposals submitted and evaluated, at least 2 FPA proposals are expected to be selected. The JU estimates that an EU contribution of between EUR 20 and 25 million for a first SGA, per selected FPA, would allow starting the

[6] The expansion of existing pilot lines will cover all the costs of extending the existing pilot lines to include quantum-specific features and their operation as quantum pilot lines.

expected outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of an FPA proposal indicating different amounts for a first SGA.

2.3.1.2 Scope

The aim is to support two or more pilot lines implemented through a Framework Partnership Agreement establishing a stable and structured long term partnerships between the Chips JU and consortia of industry, research organisations and the institutions in quantum technologies who commit themselves to establishing, coordinating and implementing a strategic and ambitious R&I initiative for the development of innovative quantum chips, followed by an ambitious action for building and deploying pilot lines.

The partnerships will be set up through one FPA per technology platform, which will ensure the implementation of the initiative through several consecutive Specific Grant Agreements (SGAs) that will carry out the different activities in a common framework. The SGAs will be implemented as Research and Innovation Actions (RIA) or Innovation Actions (IA) in function of the concrete objectives of the action. The FPAs should be carried out in different phases, which will be triggered after the attainment of appropriate intermediate progress milestones identified by the consortia. The FPAs will permit the coordinated development of the technology, its validation and the nurturing of the ecosystem. The developments should be integrated in one pilot demonstrator per FPA to validate the developments and demonstrate the scalability potential.

The infrastructures of the pilot lines should be installed in a pre-operational environment in the facilities of the hosting entities. The FPAs and SGAs should target delivering components for building and deploying in the EU of quantum technologies based on European technology.

The FPAs are expected to pursue an inclusive approach in the development of the necessary EU-wide quantum ecosystem, ensuring European wide participation of relevant stakeholders across the EU and take-up of the technology developed.

The FPAs should include research institutes, universities, RTOs, industry, including SMEs as well as any other organization that can play a role in the realization of the objectives of the initiative.

The FPAs should describe the planned mechanisms guaranteeing that all IP generated in the initiative stays in the EU and will not be transferred to third countries, dedicating an appropriate effort to IP management, protection and exploitation (i.e. IP licensing, IP warranty, etc.).

The FPAs should present a professional project structure management, a strategic R&I roadmap to implement the activities, and governance that are appropriate to coordinate the implementation of the future SGAs, including addressing the industrial use cases, and to deliver effectively and efficiently the main results of the initiative.

The FPAs should put in place appropriate management and progress control mechanisms, in particular, the establishment milestones for the SGAs assess the correct advancement of the work towards the goals of the overall initiative.

The FPAs should establish interaction with the relevant stakeholders and pilot lines and the design platform of the Chips JU to coordinate work on horizontal issues and exploit synergies where relevant.

The FPAs are expected to achieve Technology Readiness Level (TRL) 8. The actions implemented under the first SGA are expected to achieve Technology Readiness Level (TRL) 6.

Proposals should address the following activities:

- Developing scalable production processes for quantum chips in view of building industrial production processes.
- Integrating cutting-edge Quantum Process Design Kits (PDKs) with European virtual design platforms to standardize production and reduce the need for custom developments.
- Enhancing technology (including enabling technologies) and manufacturing readiness levels across the quantum industry, addressing applications in one or more of the following: quantum computing, communications, simulation, and/or sensing.
- Establishing standardized methodologies for the design, test, and manufacturing of quantum chips to streamline production processes and broaden the application sectors.
- Demonstration of scalable, efficient, and stable production capabilities, aiming at high yield[7]. The development of robust and repeatable manufacturing processes tailored to quantum chips' unique requirements, enabling a consistent and reliable supply for European stakeholders.
- Developing reliable characterization tools to ensure quality assurance of quantum chips, ensuring consistency and reliability across production batches, and demonstrating the scalability of pilot line technologies from small-to-mid volume fabrication to potentially large-scale industrial production.
- Define a technology roadmap and implementation plan towards industrialisation of the production of quantum chips.

2.3.1.3 Expected Outcomes

- At least two pilot lines for quantum chips, resulting in enhanced infrastructure capable of high-yield production of quantum chips, integrating various technologies.
- Sustainable pilot lines open to European stakeholders, including SMEs and start-ups, across the whole value chain, from materials to applications, enabling technologies, and thereby creating a community of interest for those technologies.
- Advanced manufacturing techniques and integration processes tailored to the needs of the quantum industry, aiming for significant improvements in production stability and yield rates, contributing to a more reliable supply chain for quantum chips in Europe.
- A sustainable and open-access pilot line framework, significantly boosting the innovation capacity in quantum chip technologies and providing a competitive advantage to the European ecosystem.

[7] Yield is defined here as the proportion of functional components to total components within the same production run.

- Enhanced collaboration and innovation within the European quantum ecosystem, fostering long-term growth and development in the sector.
- Demonstrated ability to transition from pilot production to industrial-scale manufacturing, ensuring the commercial viability of new quantum technologies.

The pilot lines can be physically located at one or distributed over several hosting sites. A hosting site is the physical facility at which a hosting entity will host a pilot line and which is established in a Participating State that is a Member State. Proposals shall include the members that will host and develop the pilot lines for the whole duration of the SGAs.

Collaborative efforts should be clearly outlined, demonstrating how the pilot lines will build on European quantum initiatives and contribute to the broader quantum technology ecosystem. This includes synergies and cooperation with the experimental pilot lines QU-PILOT and QU-TEST of the Quantum Flagship Initiative, for R&D support, and leveraging competencies across Europe to enhance the pilot lines' capabilities and outputs.

Proposals should exhibit a robust collaboration framework that integrates efforts across academia, industry including SMEs and start-ups, and existing quantum initiatives. Successful consortia should look for collaborations and synergies with other quantum technology projects and pilot lines. Consortia should promote the reusability of developed enabling technologies and methods, enhance the scalability of solutions, and foster a cohesive and innovative quantum technology landscape across Europe.

The pilot lines should aim to significantly accelerate industrialization and time-to-market resulting in a competitive advantage for the European quantum chips ecosystem. Proposals should also develop concrete industrialization plans, providing a roadmap for the transfer of elements or all of the process technology to industrial partners in their deployment of mass-production facilities.

Proposals should include for the FPA an overall plan for the development of this pilot line subdivided in phases and explaining for each phase the objectives, expected results, the needs in terms of equipment, estimates of required person months.

Proposals should clearly highlight important milestones and identify quantum specific, and ambitious KPIs (e.g. yield, quality of the quantum chips, reliability, reproducibility, high performance, and scalability of the production, etc...) that shall be met during the implementation of the pilot line. Technology and manufacturing process risk management plans for realistic and time-bound implementation should be also included in the proposals.

2.3.1.4 Admissibility

Admissibility conditions are described in Annex 1 “HORIZON Europe conditions applicable to Chips JU” of the WP General Annexes.

Regarding page limits:

Chapter	FPP Phase
Excellence	60 pages
Impact	100 pages
Quality and efficiency of the Implementation	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

2.3.1.5 Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions:

Size limit	50 Participants

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to restrictions for the protection of European communication networks.

Participation is limited to legal entities established in EU Member States, Norway, Iceland, Associated Countries, OECD and Mercosur countries (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled by a non-eligible country or by a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees provided by their eligible country of establishment, that their participation to the action would not negatively impact the Union's strategic assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

2.3.1.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

2.3.1.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.3.1.8 Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.3.1.9 Score

The scores will be given with a resolution of one decimal.

Criteria	Range	Weight (**)	Threshold (*)
Excellence	0-5	1.0	3
Impact	0-5	1.5	3
Quality and efficiency of the implementation	0-5	0.7	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

2.3.1.10 STEP and Sovereignty Seal

This topic contributes to the objectives of the *Strategic Technologies for Europe Platform* (STEP). As such, eligible proposals that exceed the evaluation thresholds will be awarded a *Sovereignty Seal*. The Sovereignty Seal is a quality label, valid for the duration of the project, which will facilitate access to additional EU funding (alternative, cumulative or combined funding from several EU budget instruments) or national public and private investments.

2.3.1.11 Specific provisions applicable to this Call

The following points on access conditions apply.

Access conditions for pilot lines

Access to the pilot lines should be based on fair and non-discriminatory principles and should be limited to Participating States of the Chips JU, meaning EU MS, EEAs and those countries that have been associated to Horizon Europe, under which the pilot lines are funded. In determining access to the pilot lines for users established in any Participating State but controlled from third countries that are not Participating States of the Chips JU, the consortium must take into consideration the following two main criteria:

1. EU added value, i.e., their contribution to the objectives of the Chips Act as set out in Article 4.

2. Economic security considerations.

The above access criteria should also be duly considering other relevant provisions of the Chips Act Regulation (notably Recital 11[8], and Recital 27[9], such as for example those in relation to

8 It is a clear objective of the Union to promote international cooperation and knowledge exchange on the basis of the Union's interests, mutual benefits, international commitments, and, to the extent possible, reciprocity. Nevertheless, the infringement of intellectual property (IP) rights, the unauthorised disclosure of trade secrets, or the leakage of sensitive emerging technologies in the semiconductor sector could compromise the interests of the security of the Union. Against this background, the Commission is exploring concrete proposals to strengthen the Union's investment and export control frameworks. In addition, the Union and the Member States should cooperate with strategic partners to strengthen the joint technological and industrial leadership in accordance with applicable procedural requirements.

9 R&D within the Union is increasingly exposed to practices aiming to misappropriate confidential information, trade secrets, and protected data, such as IP theft, forced technology transfers and economic espionage. In order to prevent adverse impacts on the interests of the Union and the objectives of the Initiative, it is necessary to adopt an approach to ensure that the access to and use of sensitive information or results, including data and know-how, security and transfer of ownership of results as well as content protected by IP rights generated in connection to or as a result of actions supported by the Initiative, are protected. To ensure that protection, any actions supported by the Initiative and funded by Horizon Europe and the Digital Europe Programme should follow the relevant provisions of those Programmes, such as on participation of entities established in third countries associated with the programme, grant agreements, ownership and protection, security, exploitation and dissemination, transfer and licensing and access rights. It is possible to set specific provisions when implementing those Programmes, in particular with regard to limitations to transfers and licensing in accordance with Article 40(4) of Regulation (EU) 2021/695, and limitation of participation of legal entities established in specified associated or other third countries due to reasons based on the Union's and the Member States' strategic assets, interests, autonomy or security, in accordance with Article 22(5) of Regulation (EU) 2021/695 and Article 12(6) of Regulation (EU) 2021/694. Additionally, the handling of sensitive information, security, confidentiality, protection of trade secrets and IP rights should be governed by Union law, including Directives (EU) 2016/943 (11) and 2004/48/EC of the European

the handling of sensitive information, potential risks of infringement of intellectual property (IP) rights, unauthorised disclosure of trade secrets and IP rights, security, confidentiality, or the leakage of sensitive emerging technologies within the semiconductor sector.

Only users from organisations that can clearly demonstrate their contribution to EU added value, their alignment with European economic security shall be granted access. Users from third countries will be granted access when this is foreseen in the international obligations of the Union concerning semiconductors, as these defined in any relevant Digital Partnerships or Trade and Technology Council agreements. In this case, such users should still commit to fulfil the above access criteria.

In close collaboration with the Commission, the selected consortia will be tasked to further elaborate on the above access criteria as well as access conditions and widely publish them

Parliament and of the Council, and national law. It is possible for the Commission and the Member States to protect technology transfers for reasons related to Union and national security interests in relation to investments made in facilities falling within the scope of this Regulation in accordance with Regulation (EU) 2019/452 of the European Parliament and of the Council (12 13).

2.3.2 Supporting developing Quantum Chip Technology for stability Pilot Lines

Topic: HORIZON-JU-Chips-2025-SGA-QAC1

Type of Action	RIA
Indicative EU budget	50 M€
Mode	One stage, with submission of Full Project Proposal (FPP)
Invitation date	TBD
Deadline FPP	TBD

2.3.2.1 Context

Within the Framework Partnership Agreements (FPAs) awarded under topic Chips-QAC-1: Call for establishing Framework Partnership Agreements for developing Quantum Chip Technology for stability Pilot Lines, the selected consortia will be invited to submit a proposal that will implement the first 3 years of the action plan for providing stable pilot fabrication capabilities defined in the FPA that would foster quantum chips production and rapid innovation tailored to meet the needs of the European quantum industry over the next decade, in particular start-ups and SMEs. The testing and experimentation facilities should be fully integrated in the pilot lines, providing seamless production and testing services.

2.3.2.2 Expected outcomes.

The proposal should aim to establish stability pilot production capabilities for a first of their kind quantum technologies, where European companies, research centres and academic institutions can produce quantum chips on a stable pilot scale based on a shared cost model between users and service providers. Each of the targeted stability pilot lines should have a simple baseline process ready in 2-3 years (TBD) from start of the project and the full flow should be ready during the lifetime of the FPA that should encompass detailed industrialization plans, including a roadmap for transferring process technology to industrial partners for mass production.

The proposal should focus on developing scalable production processes for quantum chips, with the goal of establishing industrial-level manufacturing methods. This includes the integration of cutting-edge Quantum Process Design Kits (PDKs) with European virtual design platforms, aiming to standardize production workflows and minimize the need for custom developments. The initiative should seek to enhance technology and manufacturing readiness levels across the quantum industry, targeting applications in quantum computing, communications, simulations, and sensing. A key objective should be to establish standardized methodologies for the design, testing, and manufacturing of quantum chips, ensuring efficient production processes and broadening the range of applications in various sectors.

The proposal should demonstrate scalable, efficient, and stable production capabilities, with a focus on achieving high yield and consistency in quantum chip manufacturing. This will involve developing robust, repeatable manufacturing processes tailored to the unique requirements of quantum chips, ensuring a reliable supply chain for European stakeholders. Additionally, the proposal should outline the development of reliable characterization tools to ensure quality assurance, demonstrating the scalability of pilot line technologies from small-to-mid volume fabrication to large-scale industrial production. A comprehensive technology roadmap and implementation plan shall be defined to guide the industrialization of quantum chip production and ensure the sustainability and growth of the quantum industry.

2.3.2.3 Scope

The action will require expertise in the area of manufacturing flows for quantum technologies, in particular in quantum computing/simulation (for e.g. qubit fabrication), communication and sensing, and with issues regarding stability, reliability, versatility, process control including integrated testing and minimizing lead times.

The proposal should also cover: (i) the collaboration with other initiatives or programmes at regional, national, or European level; (ii) any additional financial support they may receive in their activities from relevant national or regional initiatives.

The proposal may include enabling technologies for quantum chips, namely advanced tools, components, and systems that facilitate the design, fabrication, operation, testing, and scaling of these devices.

However, it should not include activities aimed at developing other essential components or subsystems that are unrelated or not directly integrated with the quantum chips.

2.3.2.4 Admissibility

Admissibility conditions are described in Annex 1 “HORIZON Europe conditions applicable to Chips JU” of the WP General Annexes.

Regarding page limits:

Chapter	**FPP Phase**
Excellence	60 pages
Impact	100 pages
Quality and efficiency of the Implementation	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

2.3.2.5 Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions:

Size limit	50 Participants
Max Contribution per partner (% of the total EU funding)	40 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to restrictions for the protection of European communication networks.

Participation is limited to legal entities established in EU Member States, Norway, Iceland, and Israel (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled by a non-eligible country or by a non-eligible country entity, may not participate in the action unless it can be demonstrated, by means of guarantees provided by their eligible country of establishment, that their participation to the action would not negatively impact the Union's strategic assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

2.3.2.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

2.3.2.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.3.2.8 Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.3.2.9 Score

The scores will be given with a resolution of one decimal.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Excellence	0-5	1.0	3
Impact	0-5	1.5	3
Quality and efficiency of the implementation	0-5	0.7	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

2.3.2.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	**Maximum EU Contribution as % of the Eligible Cost according to HE (*)**
For profit organization but not an SME	50 %
SME (for profit SME)	50 %
University/Other (not for profit)	50 %

(*) beneficiaries may ask for a lower contribution.

2.3.2.11 STEP and Sovereignty Seal

This topic contributes to the objectives of the *Strategic Technologies for Europe Platform* (STEP). As such, eligible proposals that exceed the evaluation thresholds will be awarded a *Sovereignty Seal*. The Sovereignty Seal is a quality label, valid for the duration of the project, which will facilitate access to additional EU funding (alternative, cumulative or combined funding from several EU budget instruments) or national public and private investments.

2.3.2.12 Specific provisions applicable to this Call

The following points on access conditions apply.

Access conditions for pilot lines

Access to the pilot lines should be based on fair and non-discriminatory principles and should be limited to Participating States of the Chips JU, meaning EU MS, EEAs and those countries that have been associated to Horizon Europe, under which the pilot lines are funded. In determining access to the pilot lines for users established in any Participating State but controlled from third countries that are not Participating States of the Chips JU, the consortium must take into consideration the following two main criteria:

1. EU added value, i.e., their contribution to the objectives of the Chips Act as set out in Article 4.

2. Economic security considerations.

The above access criteria should also be duly considering other relevant provisions of the Chips Act Regulation (notably Recital 11[10], and Recital 27[11], such as for example those in relation to

10 It is a clear objective of the Union to promote international cooperation and knowledge exchange on the basis of the Union's interests, mutual benefits, international commitments, and, to the extent possible, reciprocity. Nevertheless, the infringement of intellectual property (IP) rights, the unauthorised disclosure of trade secrets, or the leakage of sensitive emerging technologies in the semiconductor sector could compromise the interests of the security of the Union. Against this background, the Commission is exploring concrete proposals to strengthen the Union's investment and export control frameworks. In addition, the Union and the Member States should cooperate with strategic partners to strengthen the joint technological and industrial leadership in accordance with applicable procedural requirements.

11 R&D within the Union is increasingly exposed to practices aiming to misappropriate confidential information, trade secrets, and protected data, such as IP theft, forced technology transfers and economic espionage. In order to prevent adverse impacts on the interests of the Union and the objectives of the Initiative, it is necessary to adopt an approach to ensure that the access to and use of sensitive information or results, including data and know-how, security and transfer of ownership of results as well as content protected by IP rights generated in connection to or as a result of actions supported by the Initiative, are protected. To ensure that protection, any actions supported by the Initiative and funded by Horizon Europe and the Digital Europe Programme should follow the relevant provisions of those Programmes, such as on participation of entities established in third countries associated with the programme, grant agreements, ownership and protection, security,

the handling of sensitive information, potential risks of infringement of intellectual property (IP) rights, unauthorised disclosure of trade secrets and IP rights, security, confidentiality, or the leakage of sensitive emerging technologies within the semiconductor sector.

Only users from organisations that can clearly demonstrate their contribution to EU added value, their alignment with European economic security shall be granted access. Users from third countries will be granted access when this is foreseen in the international obligations of the Union concerning semiconductors, as these defined in any relevant Digital Partnerships or Trade and Technology Council agreements. In this case, such users should still commit to fulfil the above access criteria.

In close collaboration with the Commission, the selected consortia will be tasked to further elaborate on the above access criteria as well as access conditions and widely publish them.

exploitation and dissemination, transfer and licensing and access rights. It is possible to set specific provisions when implementing those Programmes, in particular with regard to limitations to transfers and licensing in accordance with Article 40(4) of Regulation (EU) 2021/695, and limitation of participation of legal entities established in specified associated or other third countries due to reasons based on the Union's and the Member States' strategic assets, interests, autonomy or security, in accordance with Article 22(5) of Regulation (EU) 2021/695 and Article 12(6) of Regulation (EU) 2021/694. Additionally, the handling of sensitive information, security, confidentiality, protection of trade secrets and IP rights should be governed by Union law, including Directives (EU) 2016/943 (11) and 2004/48/EC of the European Parliament and of the Council, and national law. It is possible for the Commission and the Member States to protect technology transfers for reasons related to Union and national security interests in relation to investments made in facilities falling within the scope of this Regulation in accordance with Regulation (EU) 2019/452 of the European Parliament and of the Council (12 13).

2.3.3 Supporting developing Quantum Chip Technology for high-quality Trapped Ions Pilot Line

Topic: HORIZON-JU-Chips-2025-SGA-QAC2

Type of Action	RIA
Indicative EU budget	20 M€
Mode	One stage, with submission of Full Project Proposal (FPP)
Invitation date	TBD
Deadline FPP	TBD

2.3.3.1 Context

Within the Framework Partnership Agreements (FPAs) awarded under topic Chips-QAC-2: Call for establishing Framework Partnership Agreement(s) for developing Quantum Chip Technology for high-quality Trapped Ions Pilot Lines, the selected consortium will be invited to submit a proposal that will implement the first 3 years of the action plan for providing high-quality pilot fabrication capabilities defined in the FPA that would foster trapped-ions quantum chips production and rapid innovation tailored to meet the needs of the European quantum industry over the next decade, in particular start-ups and SMEs. The testing and experimentation facilities should be fully integrated in the pilot lines, providing seamless production and testing services.

2.3.3.2 Expected outcomes.

The proposal should aim to establish high-quality pilot production capabilities for a first of their kind quantum technologies, where European companies, research centres and academic institutions can produce high-quality quantum chips on a pilot scale based on a shared cost model between users and service providers. Each of the targeted high-quality pilot lines should have a simple baseline process ready in 2-3 years (TBD) from start of the project and the full flow should be ready during the lifetime of the FPA that should encompass detailed industrialization plans, including a roadmap for transferring process technology to industrial partners for mass production.

The proposal should establish scalable, efficient, and integrated production capacities for trapped-ion quantum technologies across Europe, enhancing their availability for computing, communication, and sensing applications. This effort should focus on creating a sustainable pilot line open to European stakeholders, particularly SMEs and start-ups, covering the entire value chain from materials to applications. By fostering a community of interest in quantum technologies and enabling the use of cutting-edge trapped-ion chips, the project will significantly boost innovation capacity, providing a competitive advantage for the European ecosystem in the global market. Key milestones should be clearly defined, with ambitious and

trapped-ion-specific KPIs such as high yield, high-quality quantum chips, reliability, reproducibility, performance, and scalability of production.

The proposal should aim to develop a robust European supply chain for trapped-ion quantum technologies, encouraging innovation within SMEs and ensuring that critical intellectual property remains within the EU. The proposal should also demonstrate high-quality production processes, emphasizing the maturation of scalable and efficient manufacturing capabilities. The integration of Quantum Process Design Kits (PDKs) shall be a key focus, ensuring that the production process is streamlined and adaptable, thus enhancing Europe's leadership in quantum technologies.

The action will require expertise in the area of manufacturing flows for trapped-ion quantum technologies, in particular in quantum computing/simulation (for e.g. qubit fabrication), communication and sensing, and with issues regarding high-quality, reliability, versatility, process control including integrated testing and minimizing lead times.

2.3.3.3 Scope

The calls for quantum pilot lines are part of the Chips for Europe Initiative, focusing on building capacities for the accelerated development of Quantum chips. The overarching goal is to accelerate the industrialization process of quantum pilot lines and reduce time-to-market, thereby enhancing the competitive edge of the European quantum ecosystem. The objective of these calls is to launch actions for those more mature quantum chips production approaches that are close to established manufacturing processes. These more mature technologies are pivotal in advancing computing, secure communications, sensing and various other sectors, and require stabilization of their production, integrating advanced Quantum Process Design Kits (PDKs) into the European virtual design platform.

In this context, these calls will serve as a vital resource for both industry and academia, facilitating the design, processing, and validation of quantum components, systems, and applications, leveraging state-of-the-art quantum technologies. The actions launched under these calls are critical for transitioning from research to scalable industrial production, ensuring the EU's prominence as a global quantum hub.

The whole initiative to industrialize quantum pilot lines in the EU will be implemented in several phases, where the current call marks the beginning of the first phase. The subsequent phase will be supported by a budget commensurate to its level of ambition in function of the progress made during the first phase, and commensurate with the objectives to be achieved.

Proposers are invited to contact their national funding agencies for information regarding the national co-funding.

The proposal may include enabling technologies for quantum chips, namely advanced tools, components, and systems that facilitate the design, fabrication, operation, testing, and scaling of these devices.

However, it should not include activities aimed at developing other essential components or subsystems that are unrelated or not directly integrated with the quantum chips.

2.3.3.4 Admissibility

Admissibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Regarding page limits:

Chapter	**FPP Phase**
Excellence	60 pages
Impact	100 pages
Quality and efficiency of the Implementation	100 pages

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

2.3.3.5 Eligibility

Eligibility conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

Specific eligibility conditions:

Size limit	50 Participants
Max Contribution per partner (% of the total EU funding)	40 %

For the partners of a Participating State that coordinates grants, specific rules may apply regarding the eligibility to national funding.

Subject to restrictions for the protection of European communication networks.

Participation is limited to legal entities established in EU Member States, Norway, Iceland, and Israel (see Annex 1 of the WP General Annexes for details).

In order to guarantee the protection of the strategic interests of the Union and its Member States, entities established in an eligible country listed above, but which are directly or indirectly controlled by a non-eligible country or by a non-eligible country entity, may not

participate in the action unless it can be demonstrated, by means of guarantees provided by their eligible country of establishment, that their participation to the action would not negatively impact the Union's strategic assets, interests, autonomy, or security (see Annex 1 of the WP General Annexes for details).

2.3.3.6 Financial and operational capacity and exclusion

Financial and operation capacity and exclusion conditions are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

2.3.3.7 Evaluation procedure

Please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.3.3.8 Award criteria.

Award criteria are described in Annex 1 "HORIZON Europe conditions applicable to Chips JU" of the WP General Annexes.

For more details, please refer to the Governing Board Decision on the evaluation and selection procedures related to the calls launched by the Chips JU (GB 2024.71).

2.3.3.9 Score

The scores will be given with a resolution of one decimal.

Criteria	**Range**	**Weight (**)**	**Threshold (*)**
Excellence	0-5	1.0	3
Impact	0-5	1.5	3
Quality and efficiency of the implementation	0-5	0.7	3
Total	0-15		10

(*) threshold applies to unweighted score.

(**) the weight is only used to establish the ranking of the proposals.

2.3.3.10 Reimbursement rate for establishing the EU contribution.

Reimbursement rates as percentages of the eligible cost according to HE.

Type of beneficiary	**Maximum EU Contribution as % of the Eligible Cost according to HE (*)**
For profit organization but not an SME	50 %
SME (for profit SME)	50 %
University/Other (not for profit)	50 %

(*) beneficiaries may ask for a lower contribution.

2.3.3.11 STEP and Sovereignty Seal

This topic contributes to the objectives of the *Strategic Technologies for Europe Platform* (STEP). As such, eligible proposals that exceed the evaluation thresholds will be awarded a *Sovereignty Seal*. The Sovereignty Seal is a quality label, valid for the duration of the project, which will facilitate access to additional EU funding (alternative, cumulative or combined funding from several EU budget instruments) or national public and private investments.

2.3.3.12 Specific provisions applicable to this Call

The following points on access conditions apply.

Access conditions for pilot lines

Access to the pilot lines should be based on fair and non-discriminatory principles and should be limited to Participating States of the Chips JU, meaning EU MS, EEAs and those countries that have been associated to Horizon Europe, under which the pilot lines are funded. In determining access to the pilot lines for users established in any Participating State but controlled from third countries that are not Participating States of the Chips JU, the consortium must take into consideration the following two main criteria:

1. EU added value, i.e., their contribution to the objectives of the Chips Act as set out in Article 4.

2. Economic security considerations.

The above access criteria should also be duly considering other relevant provisions of the Chips Act Regulation (notably Recital 11[12], and Recital 27[13], such as for example those in relation to the handling of sensitive information, potential risks of infringement of intellectual property (IP) rights, unauthorised disclosure of trade secrets and IP rights, security, confidentiality, or the leakage of sensitive emerging technologies within the semiconductor sector.

Only users from organisations that can clearly demonstrate their contribution to EU added value, their alignment with European economic security shall be granted access. Users from third countries will be granted access when this is foreseen in the international obligations of the Union concerning semiconductors, as these defined in any relevant Digital Partnerships or Trade and Technology Council agreements. In this case, such users should still commit to fulfil the above access criteria.

In close collaboration with the Commission, the selected consortia will be tasked to further elaborate on the above access criteria as well as access conditions and widely publish them.

12 It is a clear objective of the Union to promote international cooperation and knowledge exchange on the basis of the Union's interests, mutual benefits, international commitments, and, to the extent possible, reciprocity. Nevertheless, the infringement of intellectual property (IP) rights, the unauthorised disclosure of trade secrets, or the leakage of sensitive emerging technologies in the semiconductor sector could compromise the interests of the security of the Union. Against this background, the Commission is exploring concrete proposals to strengthen the Union's investment and export control frameworks. In addition, the Union and the Member States should cooperate with strategic partners to strengthen the joint technological and industrial leadership in accordance with applicable procedural requirements.

13 R&D within the Union is increasingly exposed to practices aiming to misappropriate confidential information, trade secrets, and protected data, such as IP theft, forced technology transfers and economic espionage. In order to prevent adverse impacts on the interests of the Union and the objectives of the Initiative, it is necessary to adopt an approach to ensure that the access to and use of sensitive information or results, including data and know-how, security and transfer of ownership of results as well as content protected by IP rights generated in connection to or as a result of actions supported by the Initiative, are protected. To ensure that protection, any actions supported by the Initiative and funded by Horizon Europe and the Digital Europe Programme should follow the relevant provisions of those Programmes, such as on participation of entities established in third countries associated with the programme, grant agreements, ownership and protection, security, exploitation and dissemination, transfer and licensing and access rights. It is possible to set specific provisions when implementing those Programmes, in particular with regard to limitations to transfers and licensing in accordance with Article 40(4) of Regulation (EU) 2021/695, and limitation of participation of legal entities established in specified associated or other third countries due to reasons based on the Union's and the Member States' strategic assets, interests, autonomy or security, in accordance with Article 22(5) of Regulation (EU) 2021/695 and Article 12(6) of Regulation (EU) 2021/694. Additionally, the handling of sensitive information, security, confidentiality, protection of trade secrets and IP rights should be governed by Union law, including Directives (EU) 2016/943 (11) and 2004/48/EC of the European Parliament and of the Council, and national law. It is possible for the Commission and the Member States to protect technology transfers for reasons related to Union and national security interests in relation to investments made in facilities falling within the scope of this Regulation in accordance with Regulation (EU) 2019/452 of the European Parliament and of the Council (12 13).