# RISC V Automotive Hardware Platform

## Chips JU Call 2025 IA Focus Topic 1

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**On-line Information Session**

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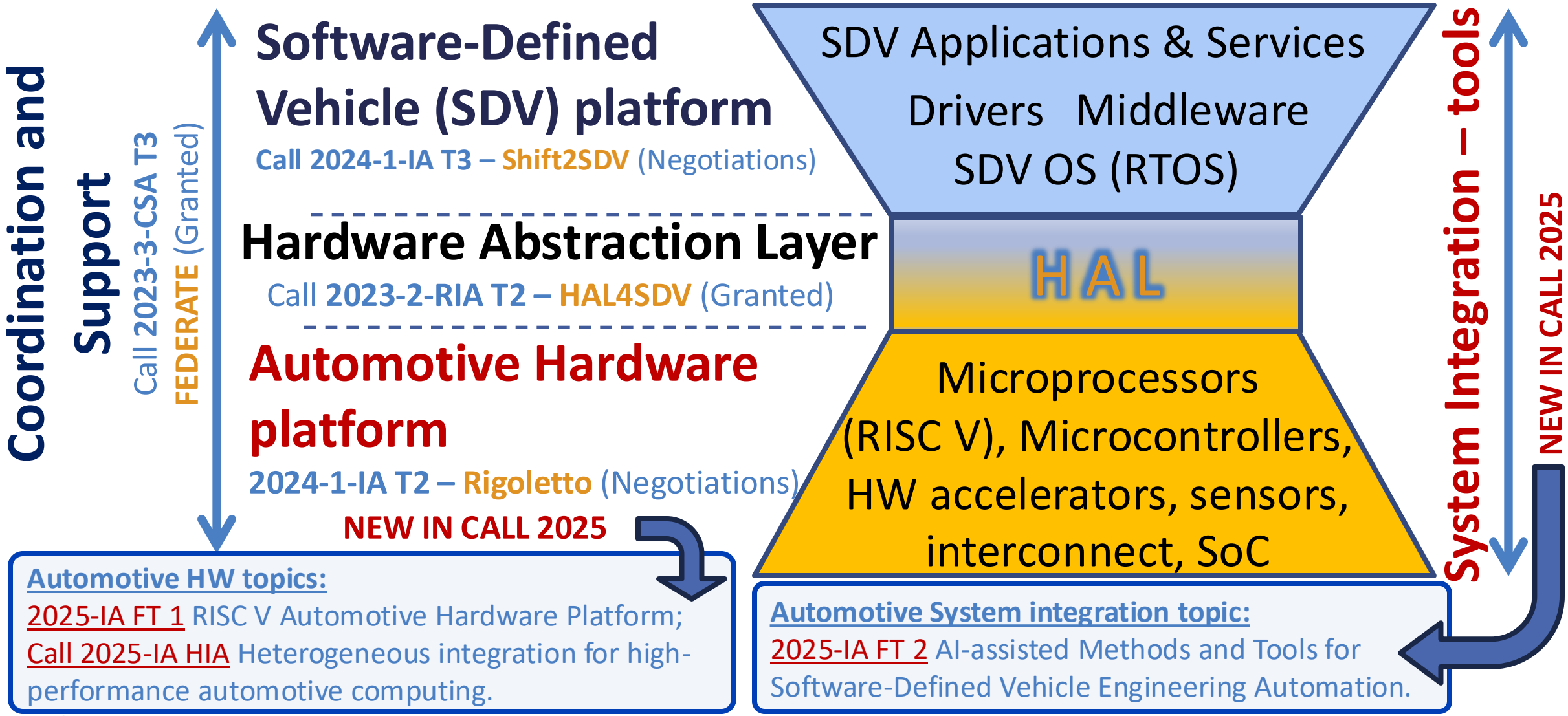
EUROPEAN PARTNERSHIP

# CHIPS JU'S VISION:

# THE VEHICLE OF THE FUTURE AS A HOLISTIC TECHNOLOGY STACK



# HORIZON-JU-CHIPS-2025-IA FT1: RISC-V AUTOMOTIVE HARDWARE PLATFORM - OBJECTIVES

**Objectives**: *translate the results of previous RISC V calls into hardware => **tape out of RISC-V** based processors/accelerators and their integration with other components such as memories using the heterogenous integration process flows developed in the other project to be funded from Call 2025-IA HIA.*

The **culmination of the project** shall include:

- **industry-grade silicon tape-out;**
- incorporating a **competitive RISC-V** application processor;
- alongside, **memory**, **accelerators** and any other relevant **IP**;
- taking advantage of **advanced packaging** techniques.

This shall be accompanied by a **mature toolset**.

# HORIZON-JU-CHIPS-2025-IA FT1:
# RISC-V AUTOMOTIVE HARDWARE PLATFORM – **EXPECTED OUTCOMES**

**Development of a high-performance automotive RISC-V reference hardware platform,** with the following **crucial components**:

- **High-Performance RISC-V Automotive Application Processors**: advanced computer **architecture**, **multi-core** configurations, **high-bandwidth memory interfaces**, catering to the **complex computing demands** of *autonomous driving systems*.
- **AI and ML Automotive Accelerators:** **specialised ISA** extensions for efficient *data-intensive computations*. These accelerators shall be optimised for automotive applications, supporting **advanced AI models** with a focus on **energy efficiency** and **real-time processing** capabilities.
- **System Integration and Interfacing:** a **coherent system** integrating **RISC-V cores**, **AI accelerators**, **memory** and system **peripherals**, including **high-bandwidth interconnects** with Quality of Service (QoS) and shared high bandwidth **cache** memories required by advanced automotive applications. System 2.5/3D integration will be developed in this programme's *call on heterogeneous integration for automotive*.
- **Software Tools and Libraries:** a comprehensive **tool-chain** to support the developed RISC-V hardware. This includes **compilers, binary utilities**, integrated development environments (**IDE**s), and **runtime libraries** tailored for automotive applications. *Hardware-software co-design* is encouraged.
- **Collaboration with the Software Defined Vehicle Initiative:** Strengthening of the **open-source ecosystem** through collaboration between hardware and software development, and automotive industry stakeholders. Alignment with *other Chips Joint Undertaking projects on the SDV* regarding **automotive standardized interfaces**, **middleware** and **API**s to facilitate **seamless integration and interoperability**.
- **Benchmarking and Quality Assurance**: techniques to assess the **performance**, **safety**, and **security** of the RISC-V platforms to ensure **compliance with automotive industry standards** and **regulations**.

# HORIZON-JU-CHIPS-2025-IA FT1: RISC-V AUTOMOTIVE HARDWARE PLATFORM – SCOPE (1/2)

**Europe's technological sovereignty in automotive processors and accelerators.**

Proposals should address:

- **high-performance RISC-V** automotive application processors;
- **artificial intelligence** (AI) and **machine learning** (ML) automotive accelerators.

**Purely pre-competitive action BUT:**

- with a clear perspective towards eventual **commercialisation** by **European industry**.
- **tangible silicon demonstrators** that can be deployed in an operational environment as **qualified devices**.
- clearly target the requirements of the **European automotive industry**.
- Where appropriate, consider the potential application of the aforementioned elements in **other industry verticals**.

**Call's aim: Develop a common European platform for automotive processors and accelerators.**

# HORIZON-JU-CHIPS-2025-IA FT1: RISC-V AUTOMOTIVE HARDWARE PLATFORM – SCOPE (2/2)

**A successful proposal should:**

- include processors/accelerators **taped-out** using leading-edge technologies and **multiple tape-outs;**
- present and maintain a comprehensive, medium-term **implementation roadmap** with a stringent yet achievable timeline and set ambitious milestones;
- reach **global-state-of-the-art** by the time the project concludes and eventually be **adopted by automotive OEMs** upon industrialization**;**
- define **clear KPIs** that are benchmarked against non-EU competitors for the project;
- **liaise** with the projects selected in the **two other focus topics**. The selected proposal will have to **align** its activities, roadmaps, milestones, transfer of results and IP, etc. with the selected proposal for the **call on heterogenous integration**;
- seek after **collaboration** with relevant **Chips JU projects** such as RIGOLETTO, TRISTAN and ISOLDE, and the EuroHPC FPA on **RISC-V for High-Performance Computing**;
- consider **synergies** with the **Chips for Europe Initiative** - Pilot Lines and Design Platform.

# HORIZON-JU-CHIPS-2025-IA FT1:

## RISC-V AUTOMOTIVE HARDWARE PLATFORM - SPECIFICITIES

- **Indicative EU budget**: **€80 million**;
- **Indicative National budget: Commensurate co-funding by NFAs**.
- **Type of Action: IA** (high TRL!) with RIA funding rates – see next slide;

**Specific eligibility conditions:**

- Size Limit: **35 participants**
- **SMEs**' share: recommended **1/3 of participants**
- **restrictions** for the **protection of European communication networks** (Art. 22(5) of HE Regulation):

Participation is limited to legal entities established in **EU Member States**, **Norway**, **Iceland**, **Associated Countries**, **OECD** and MERCOSUR **Mercosur** countries

In order to guarantee the **protection of the strategic interests of the Union and its Member States**, entities established in an eligible country listed above, but which are directly or indirectly **controlled by a non-eligible country** or by a **non-eligible country entity, may not participate** in the action **unless** it can be demonstrated, by means of guarantees provided by their eligible country of establishment, that their participation to the action would **not negatively impact the Union's strategic assets, interests, autonomy, or security** (see Annex 1 of the WP General Annexes for details).

# Page Limits and Reimbursement Rates

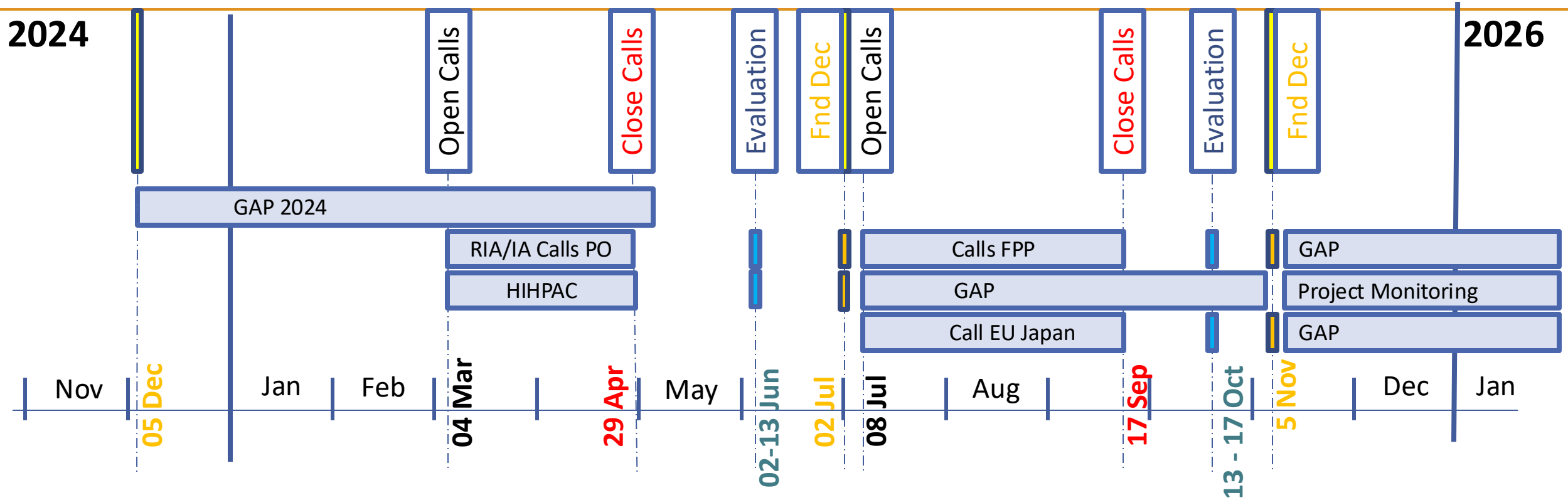
| Chapter | PO Stage | FPP Stage |
|---|---|---|
| Excellence | 60 pages | 60 pages |
| Impact | 60 pages | 100 pages |
| Quality and efficiency of the Implementation | 60 pages | 100 pages |

Proposals with more pages are admissible and will be evaluated but the pages in excess of those maxima will not be considered for the evaluation.

| Type of beneficiary | Maximum EU Contribution as % of the Eligible Cost according to HE (*) |
|---|---|
| For profit organization but not an SME | 25 % |
| SME (for profit SME) | 35 % |
| University/Other (not for profit) | 35 % |

(*) beneficiaries may ask for a lower contribution.

# TIMELINE CALLS 2025 ECS



# Questions?