Chips JU Workshop on "Microelectronics for 6G – Front End Module",

Virtual Workshop in preparation of a Focus Topic for the Chips JU WP 2026

9 September 2025, 9h15-12h30 CET

Context

Advanced microelectronics components are key to realising the 6G vision, which encompasses a wide array of functionalities, e.g. the efficient use of new frequency spectrum, AI-controlled waveforms in user terminals, joint communication and sensing capabilities as typical examples.

The 6G Smart Networks and Services Industry Association (6G-IA), representing the private side of the SNS JU, initiated several workshops and consultations since 2023 to (i) stimulate cooperation between key players from the telecoms and microelectronics domains, both from industry and research/academia, in the wake of the COREnect Roadmap[1] delivered in 2021 and (ii) identify microelectronics components of high priority for 6G where the two domains could define joint focused industrial actions to frame future promising investments.

This joint work has led to the identification of the 6G "Front End Module" (FEM), i.e. the radio reception/transmission part and traffic processing that constitutes a key and high value part of a Radio Access Network (RAN), which in itself constitutes about 80% of the value of a mobile network, as an important topic, which was the subject of a comprehensive report (early 2024), endorsed by AENEAS[2] and provided a tentative roadmap for implementation by SNS/Chips JU.

In May 2025, 6G-IA organized a follow up workshop for the definition of R&I priorities in microelectronics components for 6G where participants from both the telecoms and microelectronics domains, including industry and research organisations, reconfirmed their high interest in continuing to address the FEM activity at FR3 (7-15 GHz) as a priority frequency band with follow-up actions in future calls.

Purpose

The aim of this "Microelectronics for 6G – Front End Module" workshop is to gather detailed feedback about the needs, challenges and priorities of relevant stakeholders for a Focus Topic under consideration on the FEM extension, which is a strategic domain for 6G developments. The Focus Topic would also aim at supporting innovation in the sector and would be part of the Chips JU Work Programme 2026 in complement and synergy with the planned FEM activities under the SNS programme.

The proposed FEM extension is intended to complement the current FEM call under SNS, which will not allow to address a complete set of architectural scenarios, technological assessment and integration of all relevant modules. The starting point is that SNS activity is expected to cover a FEM detailed design for partial FR3 Operations (7-15 GHz), including beamforming and support of ICAS[3]. The timeline and effort are consistent with a 1st integration, with in-lab testing and validation carried out under controlled (e.g. cabled) conditions. It potentially allow to address two

[1] https://www.corenect.eu/roadmap

[2] Association for European Nano Electronics ActivitieS, https://aeneas-office.org/about/

[3] Integrated Communication and Sensing, a key 6G use case.

designs (e.g. CMOS and FDSOI[4] based, with e.g. GaN[5] for the RF part) but not to go for in depth testing of multiple architectures and full integration of the various modules.

As FR3 enable extreme massive MIMO[6] antenna array systems (AAS) in a compact form factor, up to 1000 antenna elements can be integrated in the same size as the current 3.5 GHz massive MIMO AAS used in current 5G networks to boosts the antenna gain. Such a dramatic increase in antenna elements require critical disruptions of the chipsets that constitute the front-end radio. The SNS call will accelerate the necessary design and validation activities at TRx level, addressing two highly relevant use cases that dimension the FEM radio design - SBFD/ISAC[7] and HBF/TDD[8]. The chipset building blocks will have to cover a plethora of functions, such as base band and data conversion (including RF DAC and RF ADC for the lower part of FR3), beam forming ICs, analog front-end ICs (Mixers/PA/LNA/TRX-Switch)[9], etc. Depending on the antenna fan-out and needed output power a combination of technologies may be envisaged. Under SNS, a small but strategic fabrication activity may be covered to make it possible to validate sub-systems and the initial integration/packaging approach. To further enable system evaluations of a scaled AAS demonstrator a follow-up action would be required.

In this context, SNS FEM call extension is critical to secure business impact for a European FEM solution targeting 6G FR3. First, because the FEM radio developed in SNS will primarily validate the RF and mixed signal chipsets – not the scaled AAS likely to integrate hundreds of TRx with more than 1000 antenna elements. Second, because the SNS call will have limitations to cater for the digital frontend development.

Against this background, the FEM extension is expected to:

i) mature the technology and subsequently, with focus on hardware development that may subsequently be valorised through IP/PoC[10] developments in the mobile communications context in connection to the system development. Typical technologies to address include Power amplifier and linearization, LNA, filters, Local oscillators, phase shifters and beam formers, AD/DA[11] converters, massive antenna arrays and antenna integration, packaging.

ii) higher level of integration compared to what can be achieved with the currently open SNS call and going towards TRL 7-8, and system validation, moving towards over the air demos (OTA). The AAS system integration and validation is particularly critical in that respect;

iii) the focus on integration aspects should eventually be connected to the APECS[12] pilot line and AAS PoC development. This would, in practice, extend the ambition and support demos of system functions over-the-air related to most opportunistic scenario, including ISAC and full-duplex;

iv) possible future to Innovation Action(s) (IA) supporting projects at high TRL level (7-8) aiming towards industrial-scale integration and/or manufacturing.

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[4] CMOS: Complementary Metal-Oxide-Semiconductor; FDSOI: Fully Depleted Silicon On Insulator

[5] GaN: Gallium Nitride

[66] Multiple Input, Multiple Output

[7] Sub Band Full Duplex/Integrated Sensing and Coms

[8] Hybrid Beamforming/Time Division Duplex

[9] DAC: digital to analog conversion ; ADC: analog to digital conversion; IC: integrated circuits; PA: Power Amplifier; LNA: Low Noise Amplifier; TRX: Transmit-Receive;

[10] IP: Intellectual Property blocks ; PoC : Proof of concept

[11] Analog to Digital/Digital to Analog

[12] Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems

Structure and expected outcome of the workshop

The workshop will be structured in two sessions: the first one centred on FEM semiconductor enabling technologies and R&I requirements that are needed to secure the technological basis to develop a FEM; the second one centred on integration/validation aspects, PoC developments and pre-industrialisation through use of Pilot lines.

Each one of them will include:

i) Presentation of the proposal for FEM extension.
ii) Feedback round from participants (telecoms and microelectronics industry representatives, RTOs).
iii) Views of the Chips JU industrial associations (AENEAS, INSIDE[13], EPoSS[14]) and of Participating States.
iv) Wrap up and conclusions focusing on the elements needed for a draft focus topic on a FEM extension.

AGENDA	Topic	Speakers
9:15– 9:50	Welcome and Introduction	Members of Chips JU and SNS JU
9:50 – 11:00	FEM topic – part 1: FEM semiconductor enabling technologies and R&I requirements	**Presentation** by supporting organisations (tbc, 15 min) Feedback and open discussion (55 min)
Members 11:00-11:15	Break	
11:15-12:20	FEM topic – part 2: integration/validation aspects, PoC and pre-industrialisation through Pilot lines	**Presentation** by supporting organisations (tbc, 15 min) Feedback and open discussion (50 min)
12:20-12:30	Conclusions	**European Commission /Chips JU**

[13] https://inside-association.eu/
[14] https://www.smart-systems-integration.org/