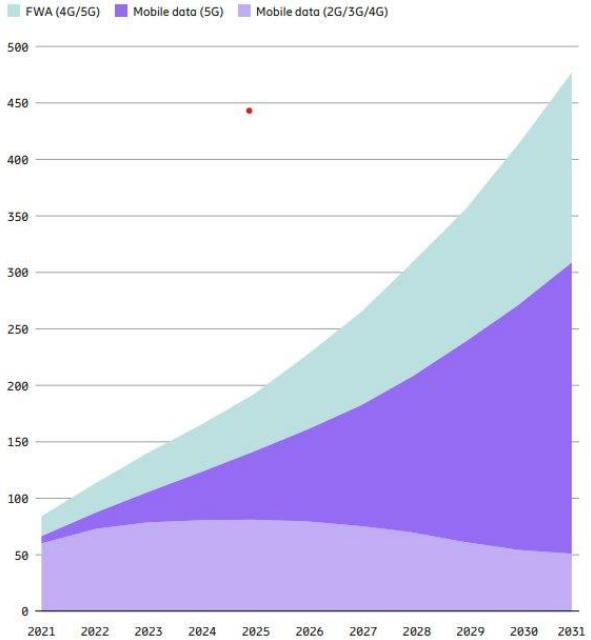
RF GaN-on-Si for 6G Front End Module applications

Info day Chips JU Call, July 2nd 2026

Joris Van Driessche, Portfolio Director RF technologies

Mobile data traffic keeps on growing

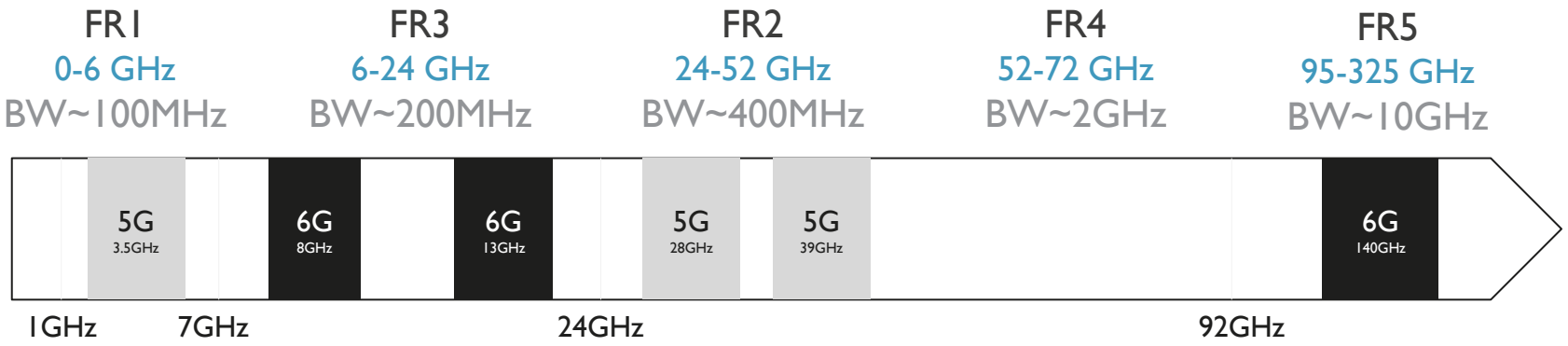
- Top Drivers
  - Smartphone video
  - FWA broadband
  - Communication services (uplink-heavy, interactive e.g video calls)
  - AI/AR glasses + AI agents
  - Enterprise cloudified work + 5G laptops (always-on mobile connectivity)
  - Autonomous vehicles/drones/humanoid droids (long term)



Ericsson mobility report, November 2025

Higher bandwidths at higher frequencies...

FR=frequency range



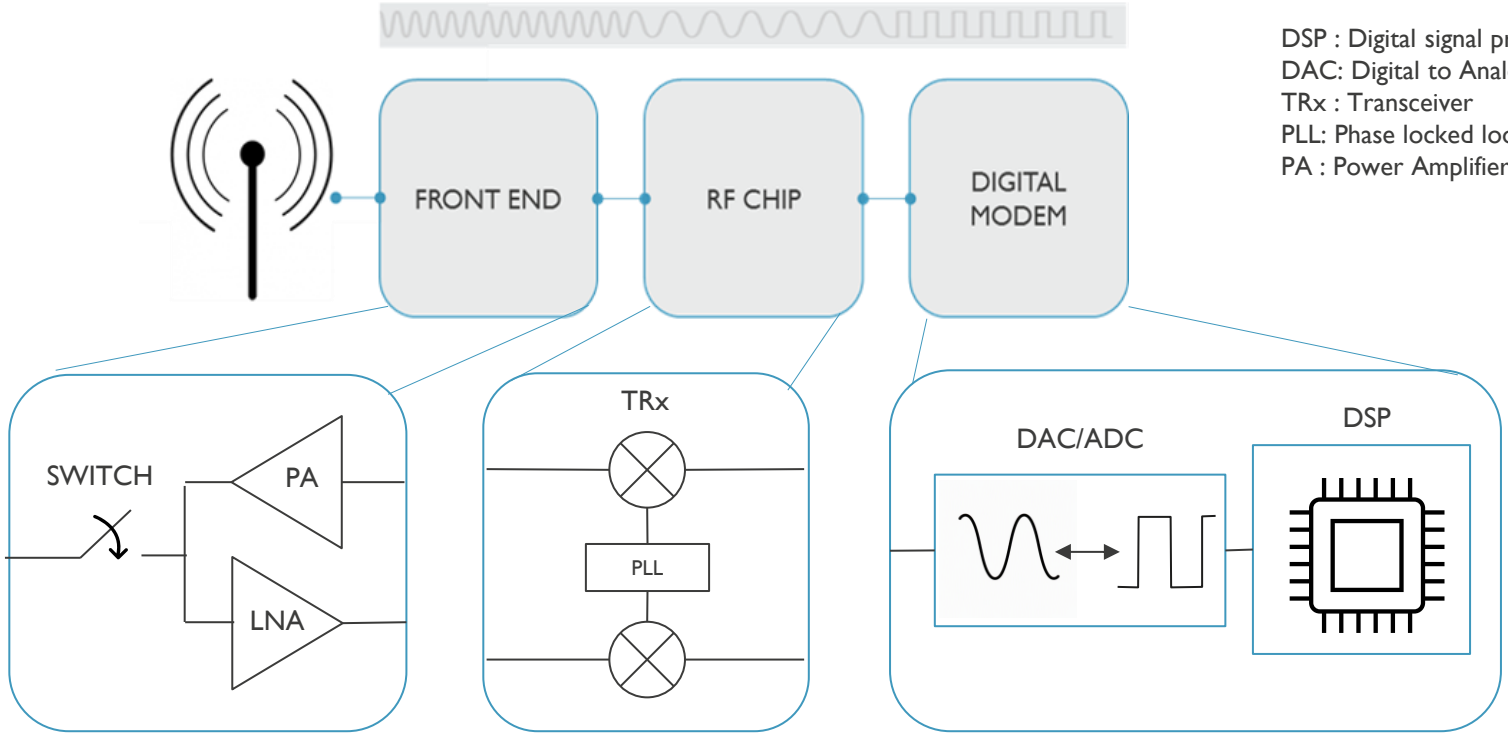
WRC23 - Candidate bands FR3:

- 6.425–7.125 GHz
- 7.125–8.4 GHz (identified for future study)
- 14.8-15.5 GHz (identified for future study)

FCC:

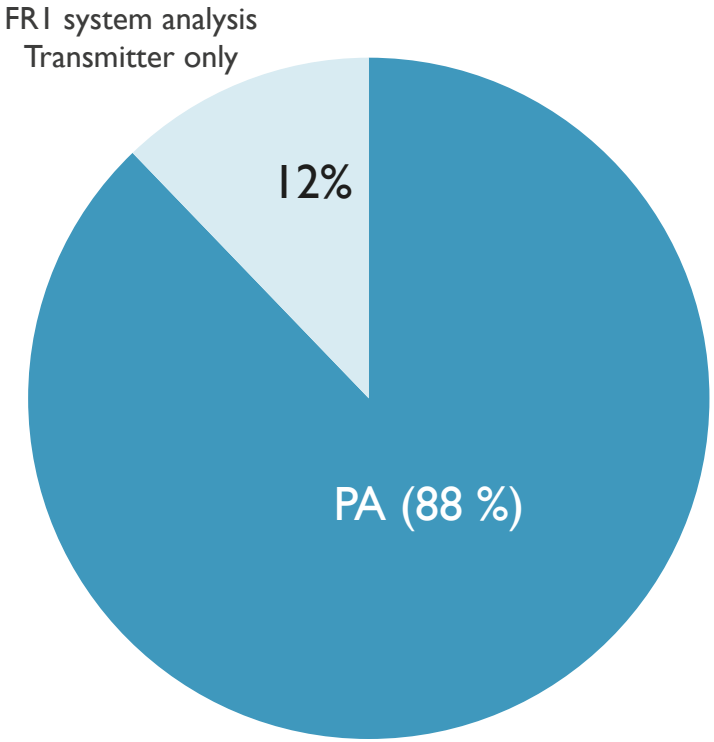
- 12.7-13.25GHz (US only)

Challenges from baseband to antenna to tackle higher frequencies



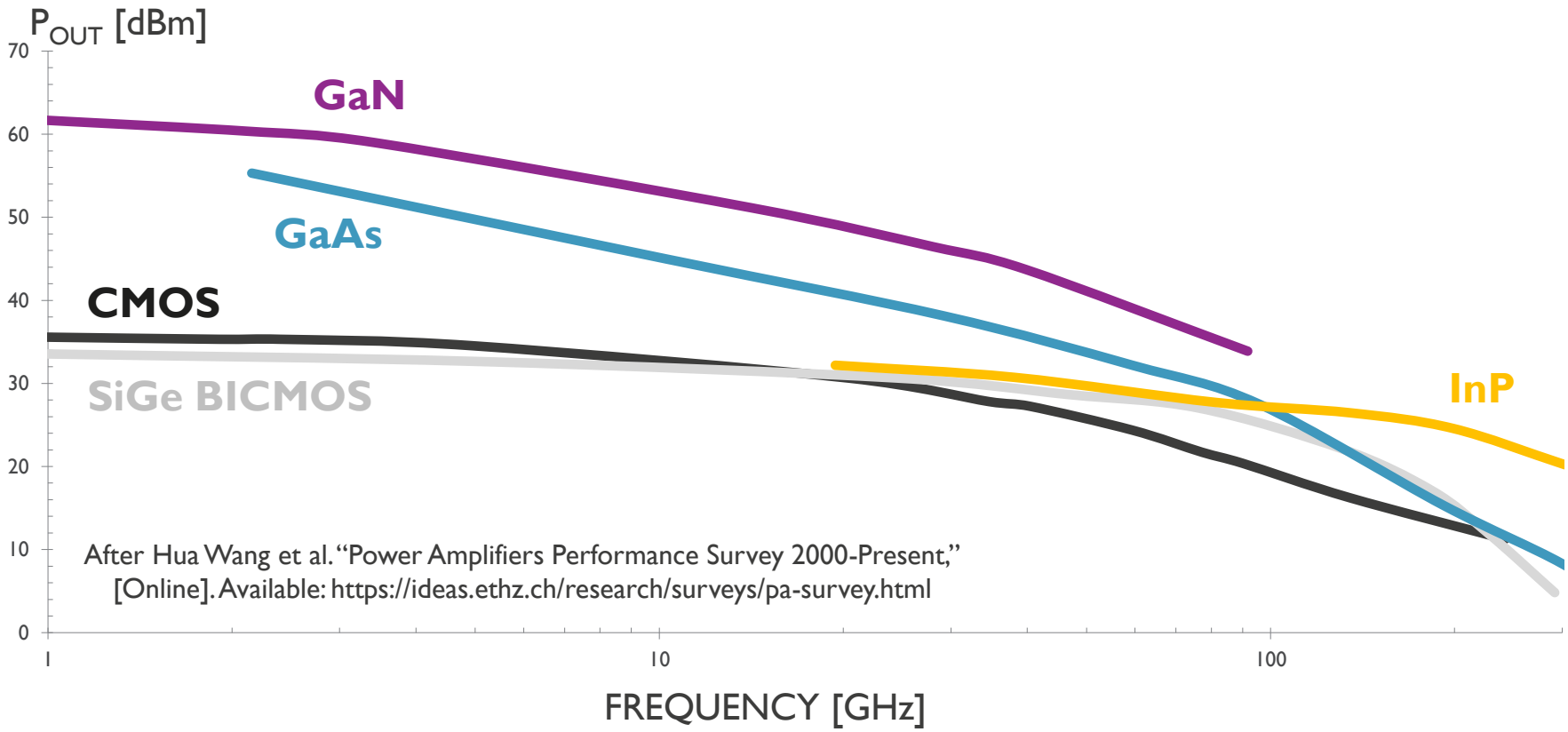
DSP : Digital signal processor
DAC: Digital to Analog Converter
TRx : Transceiver
PLL: Phase locked loop
PA : Power Amplifier

Power, efficiency & cost are the key challenges at higher frequencies



- Total power consumption is heavily dominated by the RF-FEM transmitter (TX) and more particularly by the power amplifiers (PA)
- Becomes even more challenging at higher frequencies, longer distance and for footprint restricted use cases

III-Vs are champions in power *and efficiency (not shown)*



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GaN-Si is the most cost-efficient and scalable flavor of GaN

GaN-on-GaN

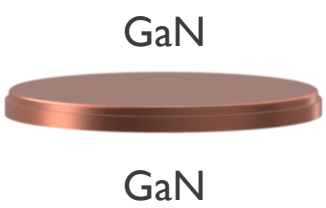
- 2 & 4 inch
- €€€

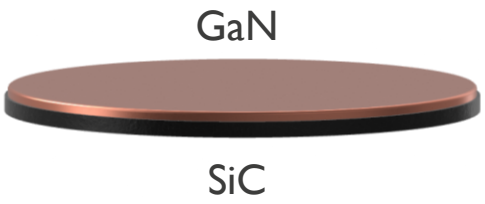
GaN-on-SiC

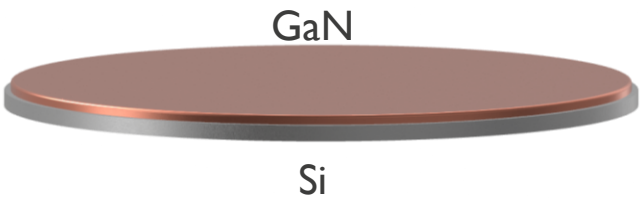
- 4 & 6inch
- €€

GaN-on-Si

- 8 & 12inch
- €

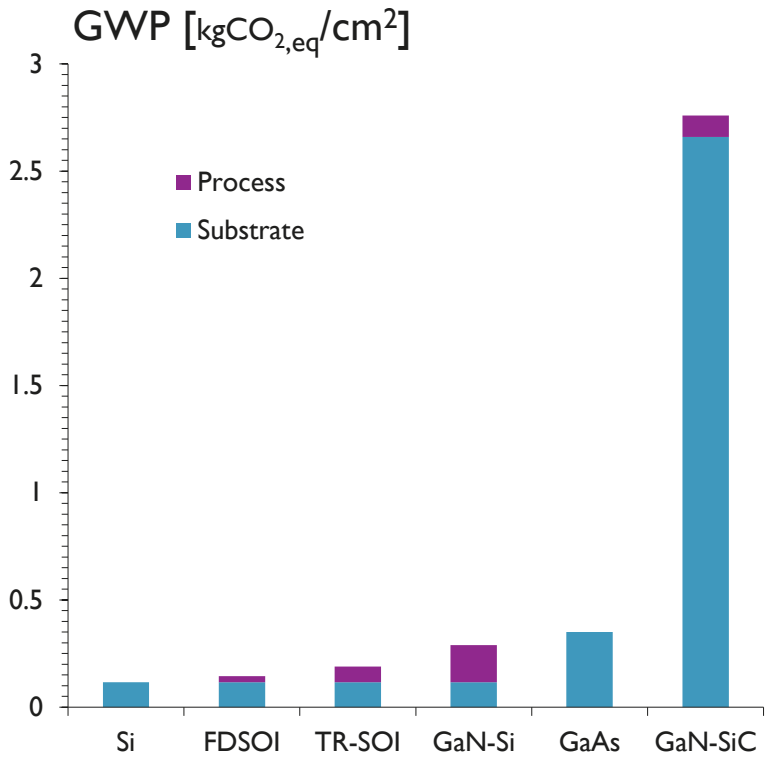


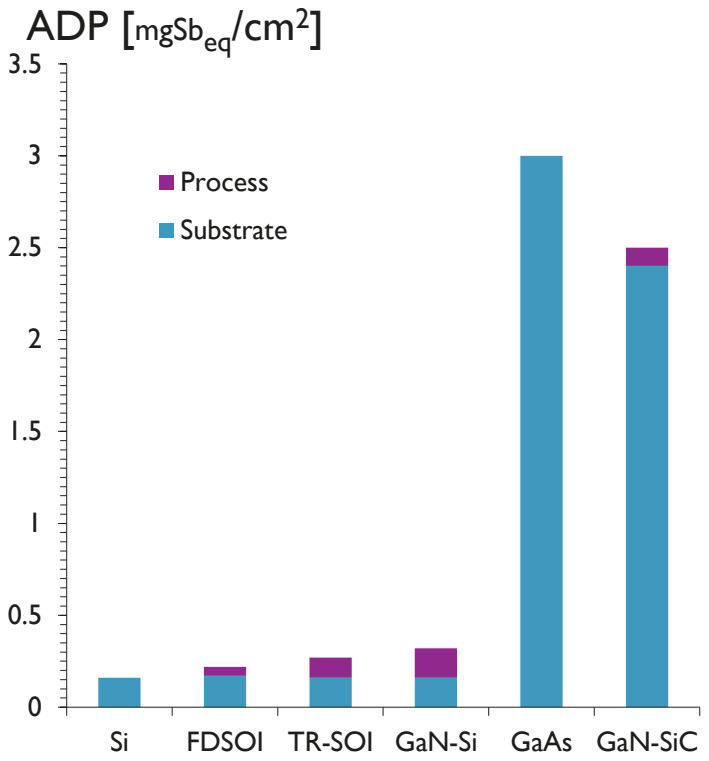




But also the most eco-friendly

B. Vanhouche et al., Electronics Goes Green 2024.



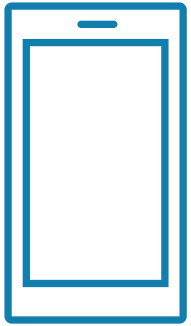


From infrastructure to handsets (User Equipment)

INFRASTRUCTURE

- High-power: ≤ 28V
- D-mode

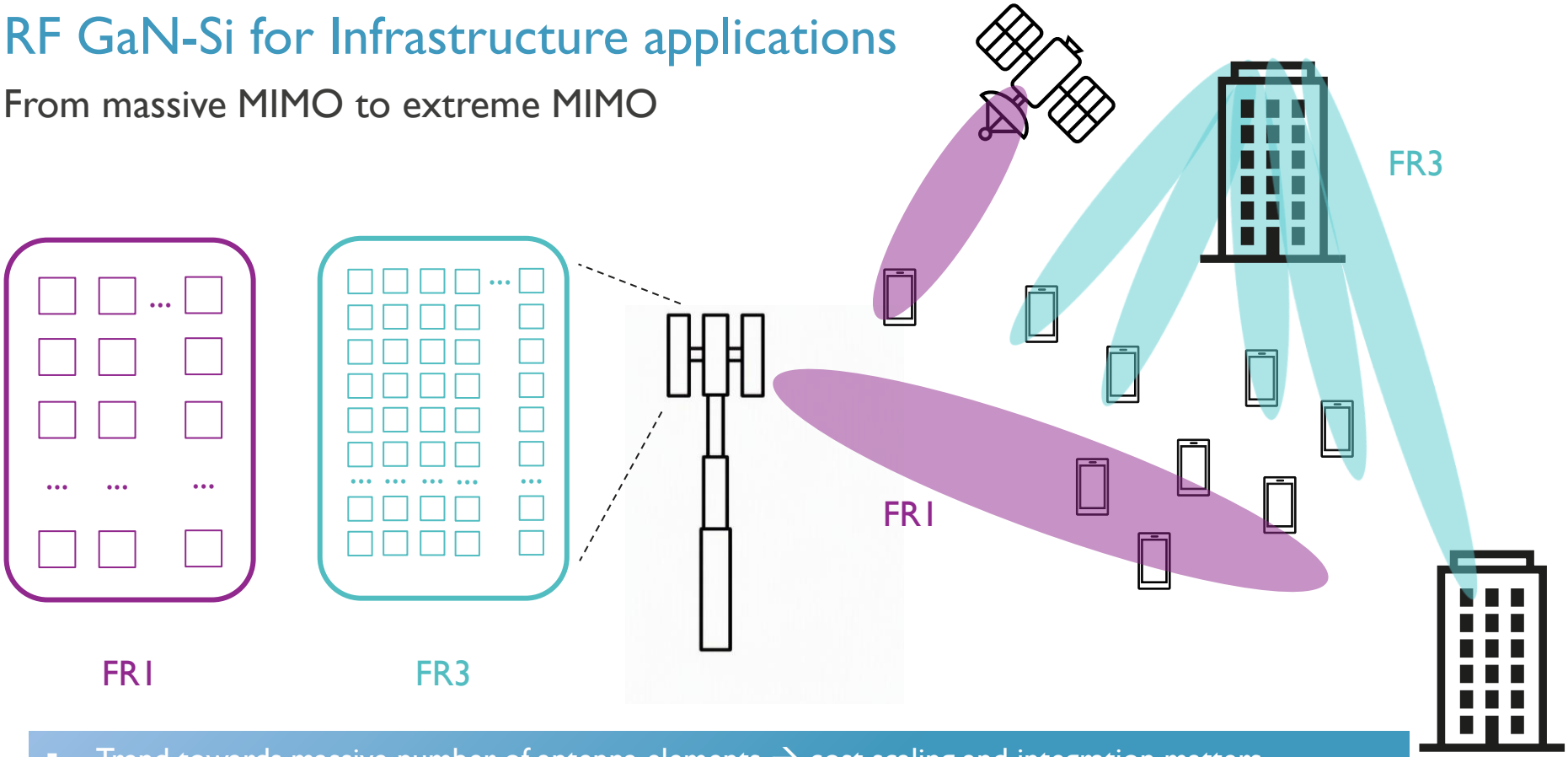
HANDSETS (UE)



- Low/medium power: ≤ 5V
- E-mode

RF GaN-Si for Infrastructure applications

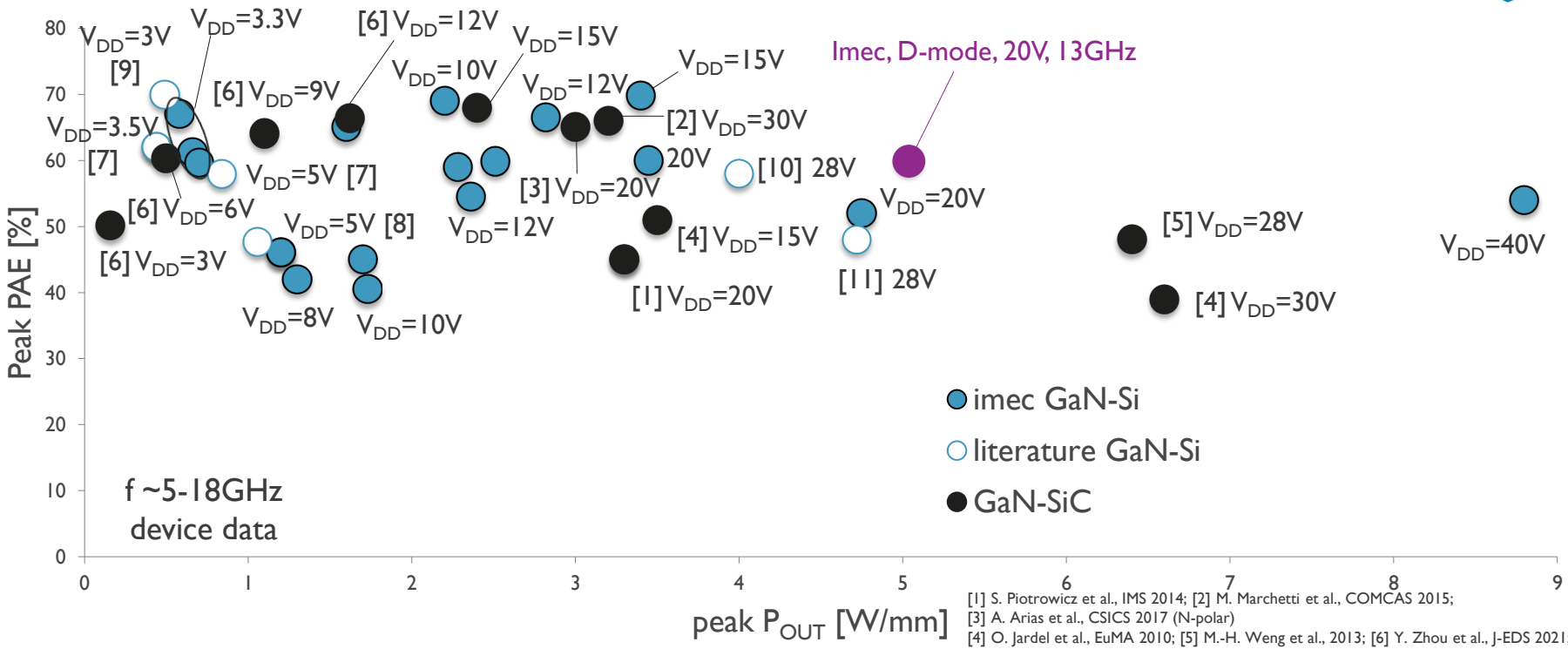
From massive MIMO to extreme MIMO



- Trend towards massive number of antenna elements → cost scaling and integration matters
- Requirements fit well with RF GaN-Si

Device performance at 5-18GHz: GaN-Si vs GaN-SiC

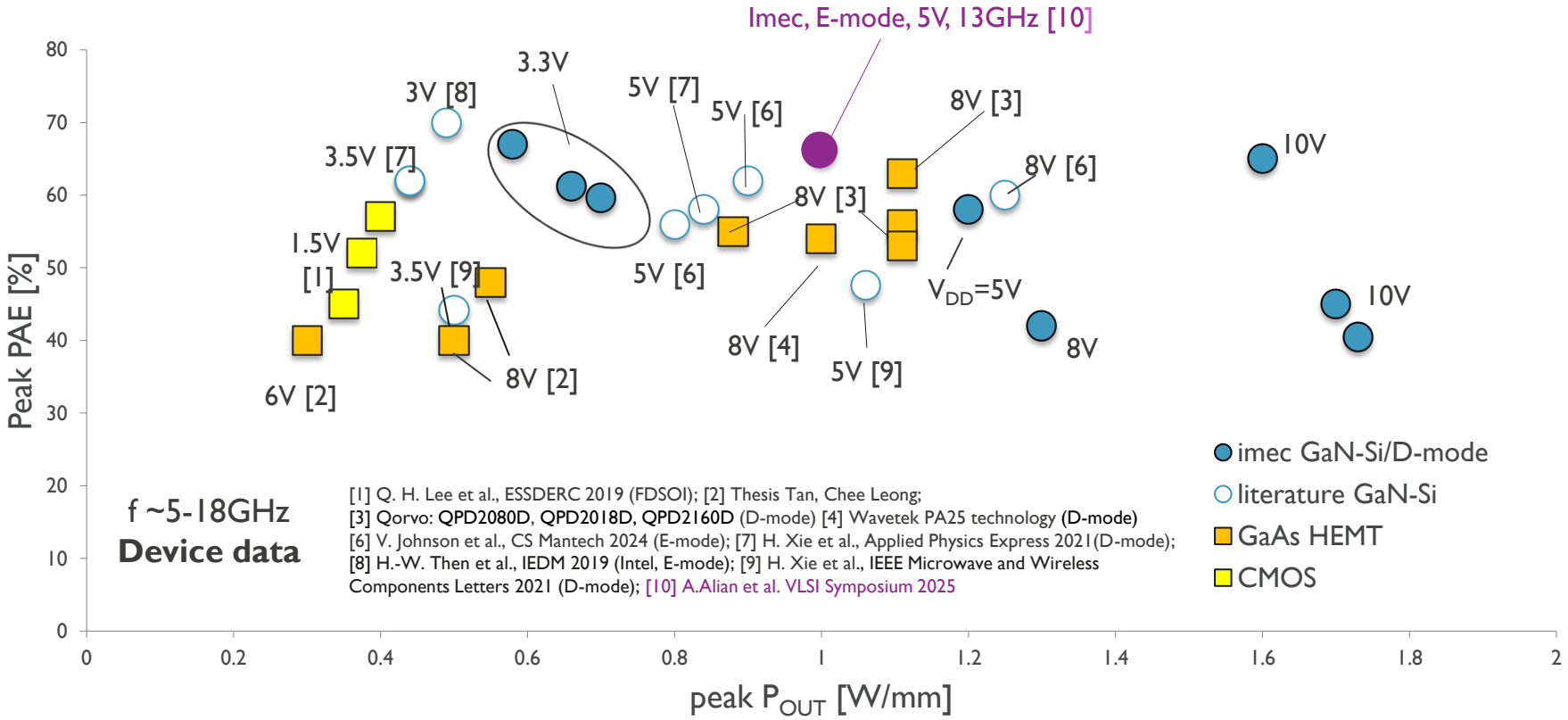
FR3 Infrastructure applications



[1] S. Piotrowicz et al., IMS 2014; [2] M. Marchetti et al., COMCAS 2015;
[3] A. Arias et al., CSICS 2017 (N-polar)
[4] O. Jardel et al., EuMA 2010; [5] M.-H. Weng et al., 2013; [6] Y. Zhou et al., J-EDS 2021;
[7] H. Xie et al., Applied Physics Express 2021; [8] H. Xie et al., IEEE Microwave and Wireless Components Letters 2021; [9] H.-W. Then et al., IEDM 2021; [10] J. LaRoche et al., CS Mantech 2012 (Raytheon); [11] J. LaRoche et al., CS Mantech 2016.

FR3 E-mode devices at 5V with P_{sat}=1W/mm and >60% PAE

Handset applications



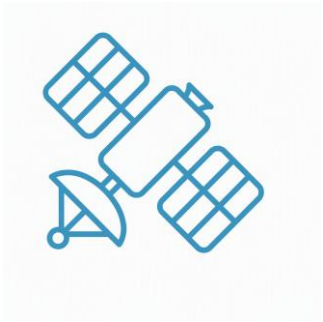
f ~5-18GHz
Device data

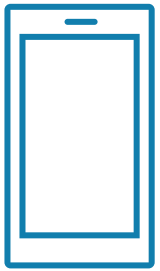
[1] Q. H. Lee et al., ESSDERC 2019 (FDSOI); [2] Thesis Tan, Chee Leong;
[3] Qorvo: QPD2080D, QPD2018D, QPD2160D (D-mode) [4] Wavetek PA25 technology (D-mode)
[6] V. Johnson et al., CS Mantech 2024 (E-mode); [7] H. Xie et al., Applied Physics Express 2021(D-mode);
[8] H.-W. Then et al., IEDM 2019 (Intel, E-mode); [9] H. Xie et al., IEEE Microwave and Wireless Components Letters 2021 (D-mode); [10] A.Alian et al. VLSI Symposium 2025

Conclusions

RF GaN-Si addresses challenges for next-generation high-performance >6GHz applications

- The continuing growth of mobile data traffic drives us to frequencies above 6GHz
- Cost, power and efficiency limits for >6GHz radio's can be addressed using GaN-Si
  - ≤28V D-Mode for infrastructure - cheaper and more sustainable option vs incumbent GaN-SiC
  - ≤5V E-mode for handset – higher gain and efficiency vs incumbent GaAs, especially for upper FR3 bands (>10GHz)






imec
embracing a better life

Front-End Module (FEM) for next generation radio communication systems

Chips-JU FEM-Call : July 2, 2026

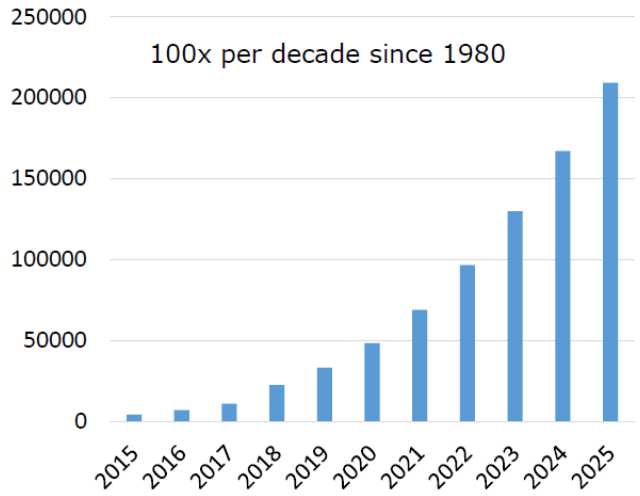
Franz Dielacher
Dielacher.external@infineon.com

OUTLINE

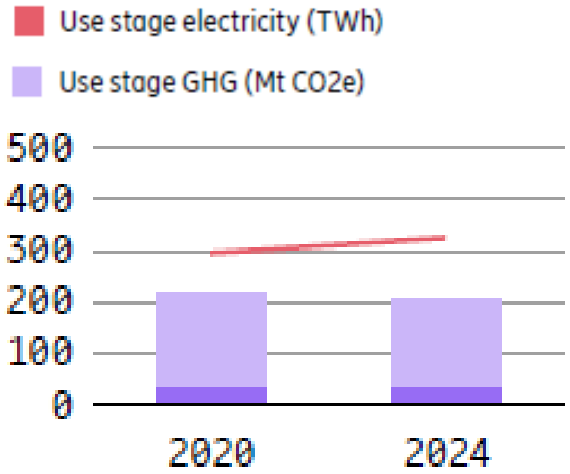
- Motivation
- FEM evolution for 6G and FR3 frequency bands
- Functional block diagram of a Front-End Module
- Semiconductor Technologies for Front-End Modules
- Heterogeneous integration of FEM
- Summary

Motivation (Network Operators View towards 6G)

Global mobile traffic (PB per month)



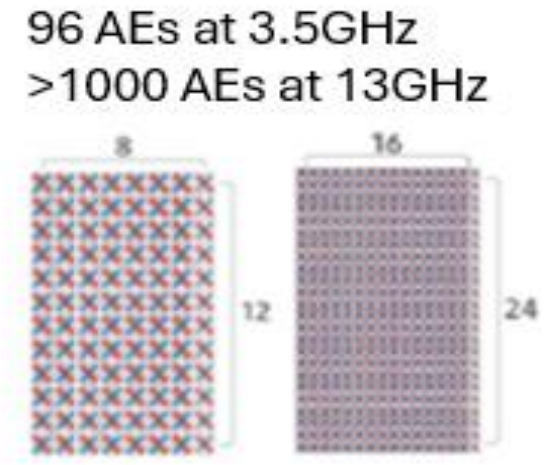
Networks energy consumption

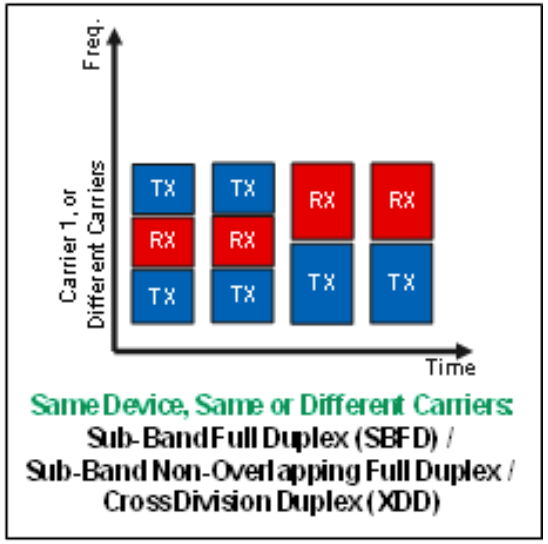


- The networks should support traffic growth and coverage at minimum cost, under energy and environmental constraints (environmental, societal and economic targets)
- Introducing new frequency bands to existing base stations has a smaller environmental impact than densifying networks by building additional base station locations.
- Spectrum in mmWave bands cannot substitute mid-bands for cost-efficient delivery of wide-area coverage and capacity
- Use Non-Terrestrial Networks for ubiquitous coverage
- Inter-system coexistence becomes imperative

Source: Ericsson Mobility Report 2025

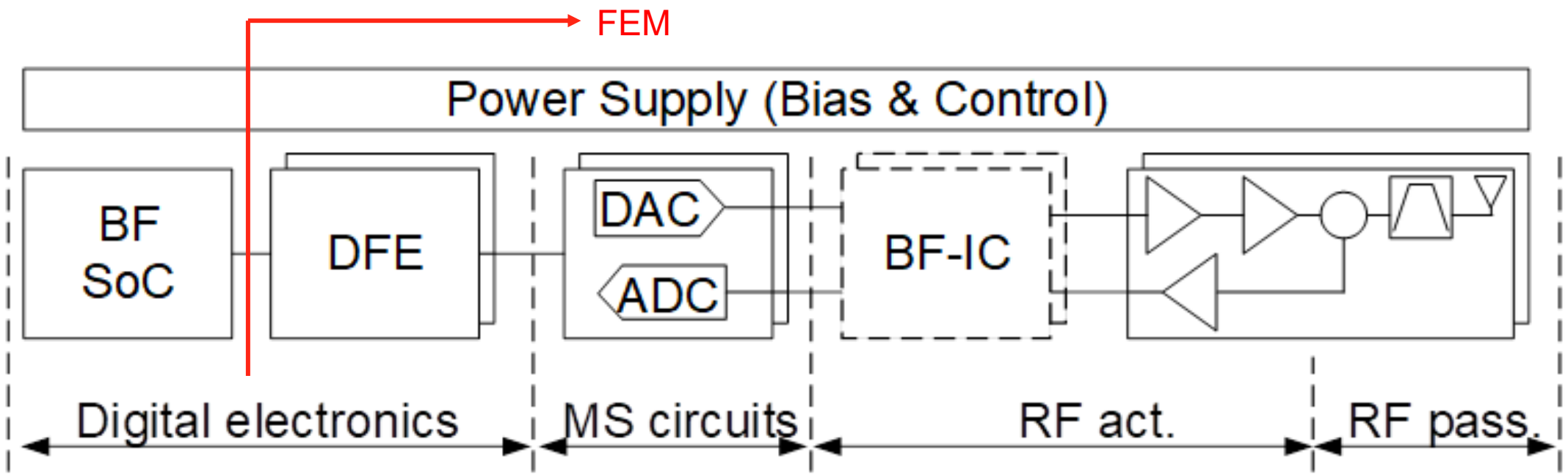
FEM evolution for 6G and FR3 frequency bands





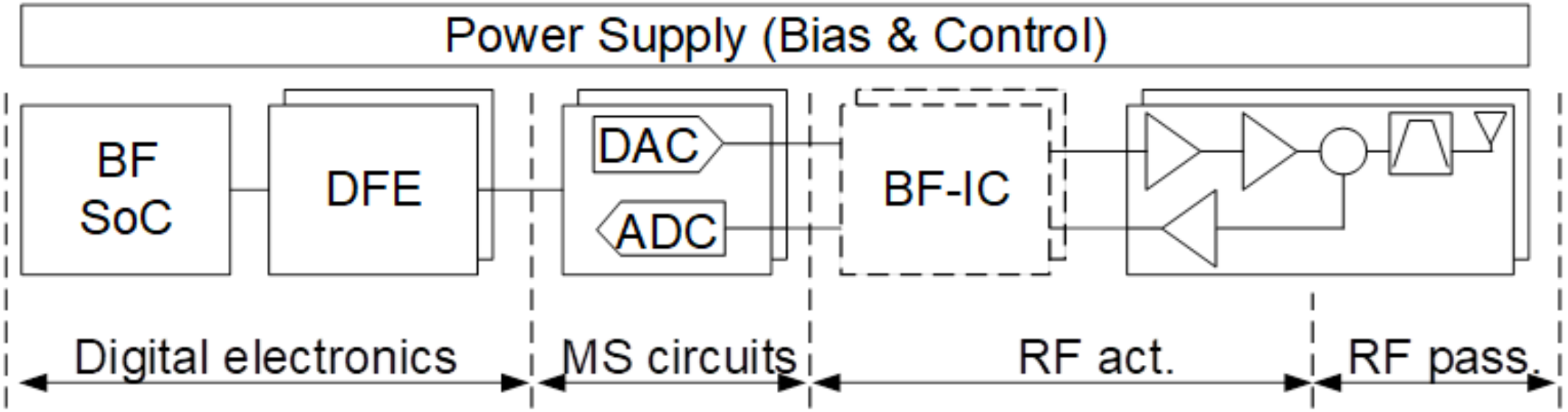
- Large arrays required for increased path loss compensation at FR3 frequencies
  - Requires very compact, low power, high efficiency FEM integration
- High bandwidth for carrier aggregation and sensing
  - Requires broadband RF transceivers
- SBFD (Sub-Band non overlapping Full-Duplex) for UL coverage extension (Rel.-19 5G-Advanced in 3GPP)
  - Requires complex interference cancellation
- ISAC (Integrated Sensing and Communications)
  - Important topics are interference management, bandwidth and waveforms
- AI/ML for channel state information and link adaptation

Functional block diagram of a Front-End Module (FEM)



- Addressing the design of a complete FEM, including a Digital Front End, a Radio Front End and Antenna
- Transmitter challenges: Power, Efficiency, Linearity, Bandwidth
- Receiver challenges: Noise, Sensitiviy, Dynamic-Range, Bandwidth
- Digital Beamforming versus Hybrid Beamforming
- RF-DAC/ADC as new architectural advancements

Semiconductor Technologies for Radio Units



- nm-CMOS (FINFET,..)
- FPGA

- nm-CMOS
- FD-SOI

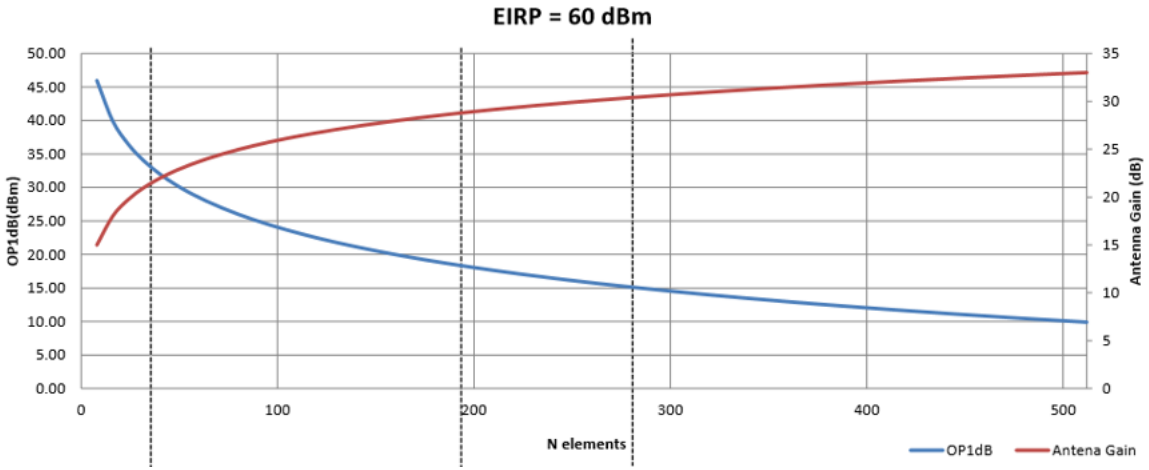
- GaN-SiC / GaN-Si
- FD-SOI, RF-SOI
-SiGe-BiCMOS

- Cavity-Filer
- Ceramic-Filter
- Circulator

BCD technology for integrated Bias & Control Unit
Hybrid integration in package – APECS pilot line
Pilot Lines for SOI, FD-SOI, nm-CMOS and WBG (NanoIC, FAMES, WBG)

Semiconductors in Antenna Arrays

Antenna Array Choices and PA technology



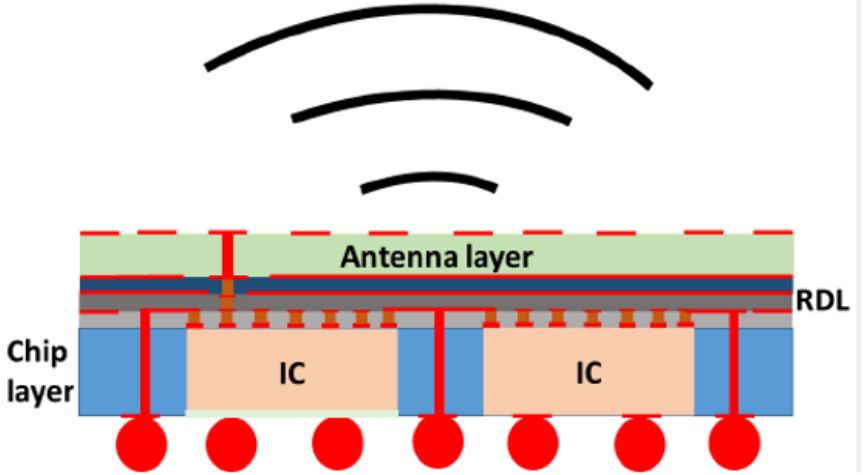
Technology comparison

Technology	DC Load line	Gain	Passives	Voltage handling	Inte-gration
GaN-SiC	++	+	+	++	-
GaN-Si	++	+	+	++	+
GaAs	+	+	+	+	0
SiGe	0	++	+	0	++
CMOS bulk	-	++	0	-	++
CMOS FDSOI	0	++	+	-	++

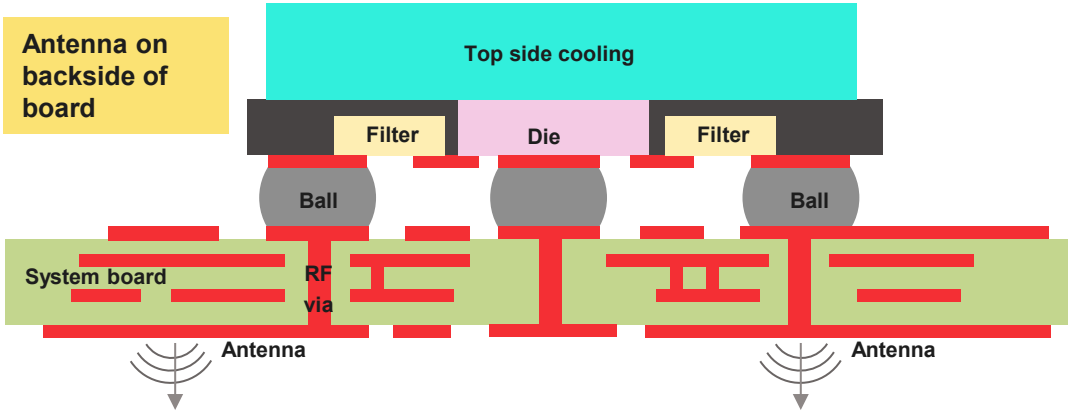
- GaN for power amplifiers and for PA/LNA/Switch integration (in GaN-on-Silicon)
- SiGe for PA, LNA, Switch and RF integration (e.g. beamformer, mixer, amplifier, VCO, ...)
- CMOS-SOI (22 FDX) for RF, AD/DA- converters and DFE integration
- BCD technology for Bias and Control integration

Heterogeneous integration of FEM (SoC / SiP)

Face-up chip (chip embedding)



Flip-chip packaged components interfaced with antennas on PCB



Design goals (challenges):

- Integration of silicon active components + compound active components + passive components
- Low loss connections in between componens and to antenna
- PA (MMIC) integration: Linearity versus efficiency trade-off, signal-coupler for DPD loopback, ...
- Thermal management: heat degrades PA performance, requires complex cooling solutions, ...
- Cost and manufacturability, size and weight

Summary

- The demand on front-ends keeps increasing and specifically for 6G and the FR3 bands new engineering ideas and technology are needed
- Leading European R&D actors need to drive innovations in hardware and software
  - Achieving a complex co-integration of mixed technologies at wafer level or in advanced packaging to maximize efficiency
  - Take into account the complex partitioning for the expected wide variety of 6G deployments which includes also satellite, device-to-device and vehicle-to-vehicle communication
  - **Achieve a timely availability of validated hardware solutions in a strong partnership between the microelectronics and communication industrial actors**

Thank you for your attention

"Europe is not as good as many Europeans think but not as bad as most non-Europeans also believe"
Future Horizons' CEO Malcolm Penn

SNS JU 2026 FEM Call

Dr. Oana Radu, Programme Officer, SNS JU

Mr. Bernard Barani, Senior Consultant, 6G-IA

Online event, Chips JU Info Day, 2 July 2026

The Future of **European Competitiveness**

~2 years from the publication of the Draghi Report

"First – and most importantly – Europe must profoundly refocus its collective efforts on **closing the innovation gap with the US and China**, especially **in advanced technologies.**"

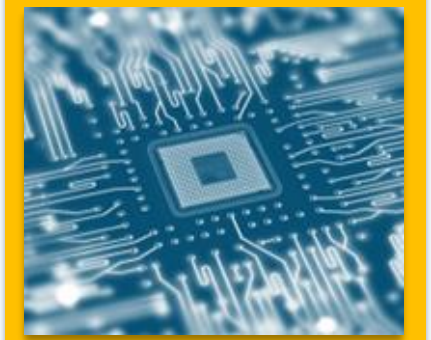
Mario Draghi

Technology Areas for EU's Economic Security

Europe's challenge is to coordinate independent layers to produce interdependent value

Quantum

Semiconductors



Artificial Intelligence

Advanced Connectivity

Biotechnology

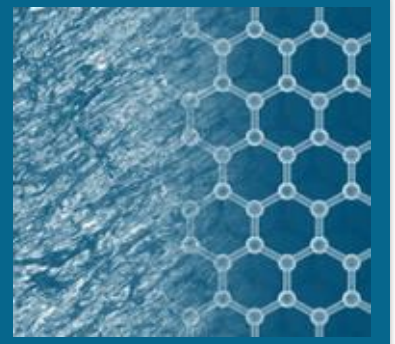
Energy

Robotics

Sensing

Space

New Materials



Align industrial, research and policy priorities at European scale

~100 Research & Innovation projects in our portfolio

Microelectronics is an important area of research for SNS JU

~618M€ of EU Public Funding Invested in SNS JU Calls

Stream A
5G Evolution Systems
- Components, Systems & Networks

Stream B
Research for Radical Technology Advancement towards 6G Definition
- System Architecture
- Wireless & Signal
- Infrastructure & Devices
- Security
- Microelectronics
- Sustainability
- International Collaboration

Stream C
Experimental Infrastructures and Platforms
- Platforms
- Enablers / Proof of Concept

Stream D
Large Scale Trials with Verticals
- Applications & Services
- Business Ecosystems

Call 1 - Started Jan '23
240M€

5G-Stardust, 6G SNS OPS, 6G SNS ICE, 6G-BRICKS, Imagine B5G, NANCY, PREDICT-6G, Across, TERA6G, SEASON, SAND BOX, 6G-XR, TARGET-X, ADROIT6G, DESIRE6G, DETERMINISTIC6G, fidal field trials beyond 5G, 6GNTN, HORSE, 6GTandem, SUPERIOT, TERRAMETA, 6Green, C6G, RIGOUROUS, 6G SHINE, HEXA-X-II, BEGREEN, TIMES, ETHER, FLEXSCALE, CENTRIC, VERGE, PRIVATEER

Call 2 - Started Jan '24
132M€

elaastic, 6G-INTENSE, INSTINCT, SEE-6G, SAFE-6G, NATWORK, 6G-REFERENCE, 6G-MUSICAL, TeraGreen, ECO eNET, 6G-EWOC, 6G4SOCIETY, 6G SENSES, 6G CLOUD, SUNRISE, GOALS, ORIGAMI, iTrust6G, OPTI-6G, ENELOPE, ROBUST-6G, FirstTo6G, 6G-XCEL, 6G TWIN, éξgence, 6G DISAC, 6G-Path, PROTEUS 6G

Call 3 - Started Jan '25
129M€

6G-Mirai, 6G-DALI, 6G-VERSUS, 6GARROW, AMAZING-6G, X-TREME 6G, FLECON-6G, AMBIENT-6G, SUSTAIN 6G, MARE, MULTIX, NexaSphere, XTRUST-6G, 6G LEADER, 6G SNS CO-OP, unity-6G

Call 4 & 5
To start in 2026
116M€

SHARC, QUEST-6G, MULTIPLY-6G, PAISE, 6GPTICON, AGENTIC6G, MAGIC-6G, 6G-CARE, PRIME-6G, PROSPERO, SIXG, 6GNTN NEXUS, SHIELD-6G, 6G-HOLONET, 6G OPTIMUS, GENIUS, PIONEERS-6G, 6G CATS, SOVEREIGN 6G, IoT-ZERO

Microelectronics in the SNS JU

Call 1: 5G Advanced and 6G projects related to microelectronics

BEGREEN
Beyond 5G
Artificial Intelligence Assisted
Energy Efficient
Open Radio Access Network

CENTRIC
AI-Native
User-Centric
Air interface for 6G networks

TERRAMETA
TERahertz ReconfigurAble METAsurfaces for ultra-high rate wireless communications

Call 2: Microelectronics-based Solutions for 6G Networks

First To6G
Fourier-Domain
TRx solutions enabling widespread realization of 6G

6G-REFERENCE
6G haRdware Enablers For cEll fRee cohEreNt Communications & sEnsing

TeraGreen
Towards Energy-Efficient Tbps Wireless Links

Call 3: Microelectronics for 6G Networks -Lighthouse

X-TREME 6G
Open µelec platform to create and design next generation chiplets and chipsets for 6G use cases.

Silicon BiCMOS, InP, and heterogenous 3D integration for high capacity radio access technologies

Resource efficient 6G algorithms and ML/AI software toolbox for computationally efficient silicon-ready baseband extensions.

Links with Chips JU

Rationale of the FEM Initiative

Consolidate **European leadership** in the radio communication domain

Competitiveness & Sovereignty	• Key for **European competitiveness** in next-generation connectivity. • **Securing a European supply chain** in the domain of **microelectronics for telecom** and networked services platforms (FEM design, integration and packaging) as **priority.**
Industrial Exploitation	• Industrial dynamics and **path to exploitation** in the context of Chips JU Pilot lines* • Stimulate **European know-how in microelectronics** components and systems for communication technologies in line with the broader objectives of the Chips Act.
Spectrum	• The strategic priority is **FR3 band**, (7–15 GHz range) and **upper 6 GHz band** (6.425–7.125 GHz) following latest RSPG recommendations and WRC 27 Agenda Items. • Versatile implementations across different ITU regions.
Use Case aspects	• Latest **progress at 3GPP** on technology and use case characteristics: reuse of cell sites, Sub Band Full Duplex, ISAC integration, 400 MHz channels, uplink emphasis. • **AI/ML applicability to FEM**. Primarily to RT implementation of radio functions. Open to other non RT functions (as appropriate). • µElectronics trade offs as a function of EU know how/capabilities and transfer towards Pilot Lines

2026 SNS JU FEM Call for Proposals is open

Check InfoDay video in SNS JU Website:

SNS JU 7th Call for Proposals - Info Day & Brokerage Event - SNS JU

Synergies and Implementation Modalities

SNS JU Call
(system aspects with PoCs at TRL 4/5)

- The linkages will be explained in the **proposal workplan**, **addressing the desired interfaces between this action at the system level and the expected Chips JU actions**
- Particular attention will be paid to:
  i) an identification of a downstream high level of node integration for further transfer to Pilot Lines (plan for transfer in scope)
  ii) the needed evolution of the design tools to support the downstream FEM development, like EDA, PDK.

Chips JU Call
(detailed design and tech choices of FEM components)

- Proposals should explain **how they plan to coordinate the project's activities with the SNS JU FEM call** and how they plan to contribute, through this project as an **intermediate step, to the final target of final system-level integration/validation** at TRL levels 7/8, including OTA testing.

Collaboration is not optional

Operational coordination SNS JU-Chips JU to capture synergies

Ongoing and recurrent **synergetic meetings**

Aligned **evaluation timelines**

Aligned use of **common evaluators**

POs to **participate as observers** in the other JU's evaluation

This collaboration will be continued in the future

For additional information

HORIZON-JU-SNS-2026-FEM-STREAM-B-02

Must Read

EU Funding & Tenders Portal

SNS JU R&I Work Programme 2026

Appendix 1: SNS 2026 Calls Overview & General Call Conditions

Important Background

General Annexes for Horizon Europe call conditions 2026-2027

List of participating countries (including RoK association to HE)

SNS JU specific provisions covering Admissibility, IKOP, Eligibility & SMEs

FAQ & Support

FAQ Call 6 – Frequently Asked Questions - SNS JU

All questions:
SNS JU contact e-mail

SNS Brokerage Platform

SNS JU **FRONT END MODULE (FEM) CALL**

Long Term Vision

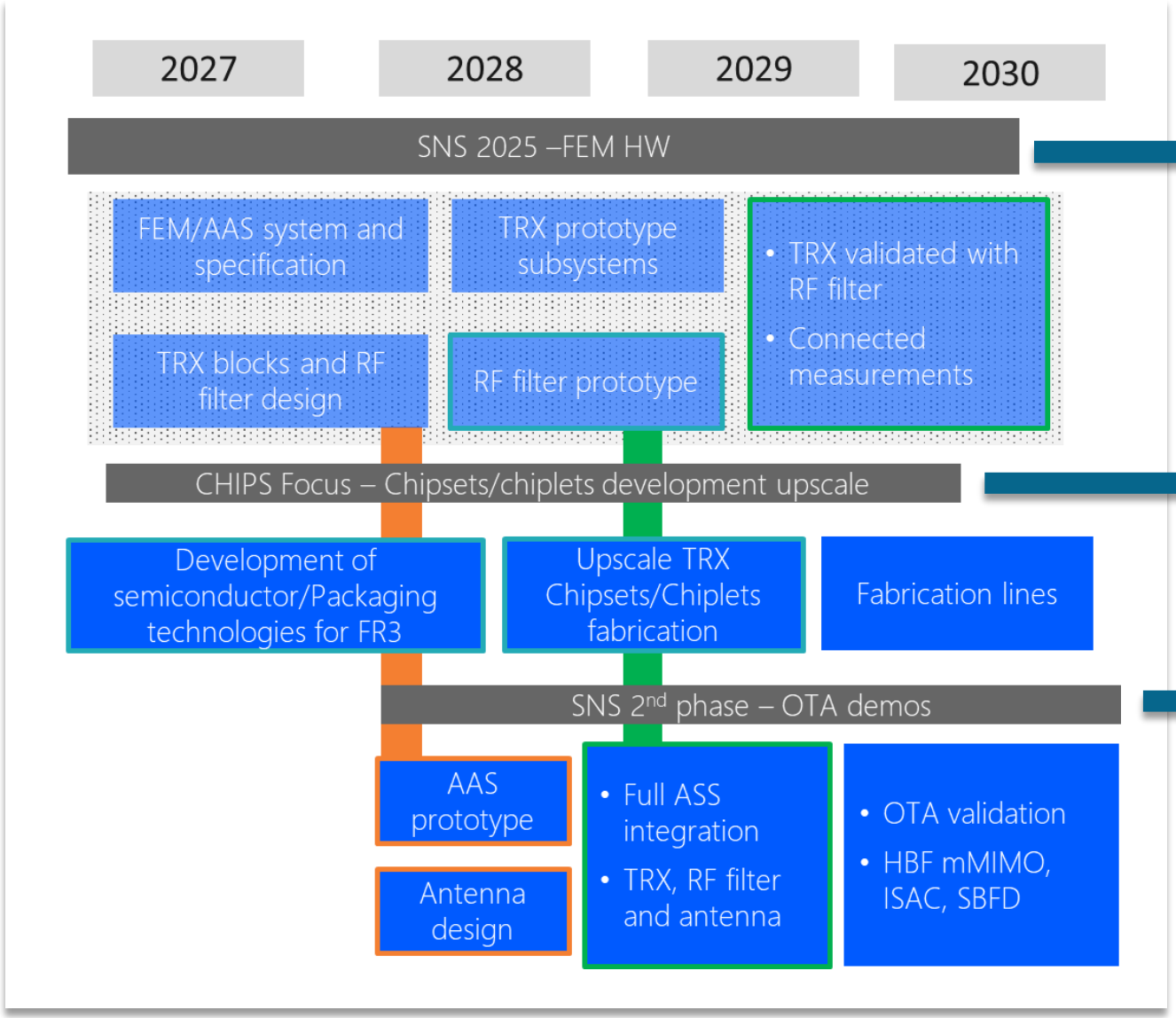
- **NOT** Business as Usual
- **Large-scale** initiative spanning over several calls across 2 JU's;
  1. **SNS JU FEM call**: System and design perspective
  2. **Chips JU call under WP 2026**: Detailed technological perspective
  3. **Last call under SNS WP 2027** (TBD/TBC): Integration and testing perspective

Key Success Factors

- **Complementarity and directionality** over the various calls
- **Strong European industry commitment** (telecom+µElectronics)
- **Industrialization target**: EU capabilities in µElec for telecoms (Chips Act)

European Sovereignty and competitiveness

Complementarities



FEM Journey approach

- **SNS phase 1** System aspects, tech trade offs, critical subsystem PoC's
- **Chips'26** detailed tech design, **upscale of chips development and integration** technologies to achieve industry grade FEM and **facilitate the evolution towards full integration/OTA validation**.
- **SNS phase 2 (TBC)** Integration, OTA testing

Multifaceted Challenges underpinning FEM Work

FR3 Band & Upper 6GHz band

- Usability of **FR3 band**, (7–15 GHz range) in Europe and the **upper 6 GHz band** (6.425–7.125 GHz) following latest RSPG recommendations and WRC 27 Agenda Items
- **Sharing** capabilities wth incumbent services
- **Versatile implementations** across different ITU regions.

Technological Issues

- **Complexity of RF Front end,** high integration level of antennas
- **Processing complexity**
- **SiP, integration** of multiple technologies from baseband to RF, **packaging**
- **AI/ML applicability** for key L1 functions.
- **µElec tech trade offs**
- **Cost, energy efficiency**

Use Case aspects

- Latest progress at 3GPP on technology and **use case characteristics**: reuse of cell sites, Sub Band Full Duplex, ISAC integration, 400 MHz channels, uplink emphasis..
- **Wideband digitization**, fast and accurate channel-select filtering , HBF for TDD systems
- AI/ML **high uplink capacity** requirements

Industrial Issues

- Stimulating **European know-how** in microelectronics components and systems for coms (Chips Act)
- Stimulating a **European supply chain** in the domain of microelectronics for telecom and networked services platforms (FEM design, integration and packaging)
- **Leveraging Chips JU Pilot lines** towards pre industrialization and exploitation

Scope of the SNS JU Call (1/3)

Scope

Complete FEM **design and architecture**, from Digital to RF modules

- **Coverage of the FR3 band with upper 6GHz**, sharing compatibility as appropriate, ITU regional variations capable;
- **ISAC capabilities**, maximisation of functional blocks;
- **Characterisation of all building blocks**, PA, LNB, BF, etc.
- **Integrated design from RF to Baseband**, taking into account ITU requirements (BW, channel width, etc.)
- **Capability for high uplink capacity** (AI/ML traffic);

Scope of the SNS JU Call (2/3)

Scope

Complete FEM **design and architecture**, from Digital to RF modules

- **Coverage of use case requirements**: FWA/cellular capability, Sub Band Full Duplex operations, secure ISAC integration.
- **Analysis and trade off technologies**: FDSOI, GaN, InP, CMOS…and their integration, also considering i) EU ecosystem capabilities; ii) Chips JU PL transfer; iii) packaging feasibility.
- **AI/ML applicability for key L1 functions**, e.g., CSI, spectrum management and I/F mitigation, non-functional properties such as energy efficiency. (indicative list).
- **AI/ML implementation aspects not suggested**.
- **Plan for transfer towards Pilot lines** and assessment of design tools/environment (EDA, PDK).

Scope of the SNS JU Call (3/3)

Scope

Other relevant aspects

- **PoC (s) for critical subsystems** in scope at TRL 4/5
- **Key 1**: Very solid **combination of European industrial leaders** in the radio coms and microelectronic domains, with a demonstrated track record and **capabilities to industrialize** and market the solution in Europe and at a global level
- **Key 2:** Contribution to the **sovereignty of the EU supply chain** in the domain of microelectronics for telecom/networked services platforms. It implies control of FEM design, implementation, and packaging with European solutions up to the prototyping level, without backdoor implementation via firmware, and full security of the final solution.

NB: Applicants should clearly identify the priorities addressed if they only cover a subset of the above scope

Expected Outcomes (1/2)

FEM DESIGN — TECHNICAL CAPABILITIES

SPECTRUM COVERAGE

FR3 (7–15 GHz, ext. to 24 GHz) + Higher 6 GHz band.
Built-in tuning for regional variations (WRC-27).

INTERFERENCE MITIGATION & SHARING

Protects incumbent FR3 users; maximises spectrum sharing aligned with the European regulatory approach.

MASSIVE MIMO & ANTENNA INTEGRATION

Supports a large number of antenna elements beyond SoA. Compensates increased path loss through massive MIMO.

RF PROCESSING CAPACITY

At least an order-of-magnitude increase in RF processing vs 5G FR1 implementations.

5G SITE REUSE & DEPLOYMENT SIMPLICITY

Enables reuse of existing 5G cell sites, minimising deployment complexity and rollout cost.

SUB BAND FULL DUPLEX (SBFD)

Concurrent, efficient SBFD implementation with minimised waveform differences and maximised common functional blocks.

INTEGRATED SENSING & COMMUNICATIONS (ISAC)

Simultaneous ISAC support with common waveform design; sensing and communication functions share maximum functional blocks.

UPLINK CAPACITY FOR NEW USE CASES

Addresses 6G requirements for greater uplink capacity serving new traffic classes and emerging use-case scenarios.

ITU IMT-2030 COMPLIANCE

Meets ITU IMT-2030 requirements: increased carrier rate, user data rate and reduced latency targets.

CELLULAR & FWA DUAL-MODE SUPPORT

Enables both cellular (FR1-like) and Fixed Wireless Access (FR2-like) deployment scenarios on a single platform.

Expected Outcomes (2/2)
INDUSTRIAL AND STRATEGIC

EUROPEAN TELECOM–MICROELECTRONICS ECOSYSTEM

Strong and lasting cooperation between European lead telecom system suppliers and microelectronics technology leaders. Stimulates a European telecom components ecosystem aligned with EU sovereignty objectives.

MICROELECTRONICS HETEROGENEOUS INTEGRATION

Low-cost, low-energy elementary constituent modules. Efficient packaging leveraging heterogeneous integration technologies where European industry holds strong expertise and know-how.

ADVANCED DESIGN TOOLS (EDA / PDK)

Stimulates availability of higher-TRL design tools including EDA platforms and PDKs (Process Design Kits), enabling a more competitive European semiconductor design capability.

INDUSTRIALISATION PATHWAY & CHIPS JU PILOT LINES

Clear roadmap toward downstream industrialisation in Europe. Leverages Chips JU pilot lines based on technology selection, creating a direct bridge between research and manufacturing.

CHIPS JU ECOSYSTEM BRIDGE

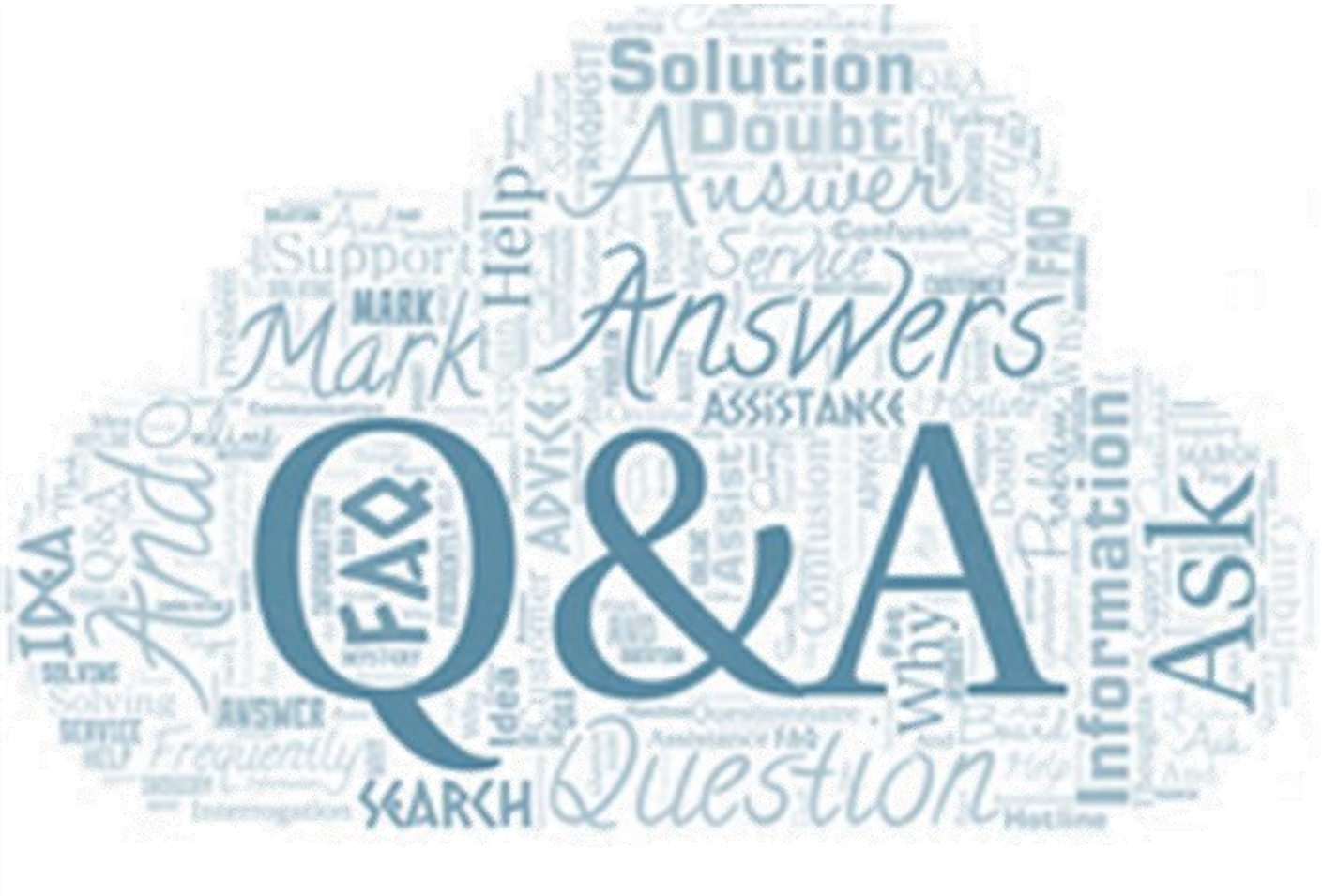
Coordinated pathway to Chips JU calls. Technology readiness trajectory designed to feed into European semiconductor manufacturing infrastructure and supply chain resilience.

APPLY AI STRATEGY — EU POLICY ALIGNMENT

Contributes to the Union's Apply AI Strategy. Positions 6G FEM research as an enabler of AI-integrated networks, aligning with EU digital sovereignty and industrial competitiveness goals.

FEM Design outcomes directly **support EU technological sovereignty** in 6G infrastructure
Connecting advanced RF engineering, microelectronics integration, and AI-ready network architectures

Q&A


Solution
Doubt
Answer
Help
Support
Service
Mark
Answers
ASSISTANCE
Q&A
FAQ
Information
Ask
Why
Idea
SEARCH
Question

The European Smart Networks and Services Joint Undertaking

View on mobile

#SNSJU

Contact us at: smart-networks.europa.eu

6G Front End Module

Information Day

Call on the 6G Front End Module

2 July 2026

Agustin Diaz-Pines
Deputy Head of Unit, CNECT E1
European Commission

Telecoms at the core of rising digital economy

The foundation of the digital economy and society

A crucial infrastructure for security and sovereignty

Dual use, safe and resilient infrastructures

The backbone of digitisation of all EU businesses

A key domain for EU economy

6,7% of EU GDP, Eurostat 2021

Booming public investments from our main competitors

Booming investments for Member States

€ 2 Billion for 6G, e.g.

A high risk, R&D intensive domain

Risk sharing with public policies/partnership

A key technology for EU policies

- EUCCS, IRIS²,
- Sustainability;

An EU valorisation platform for key technologies

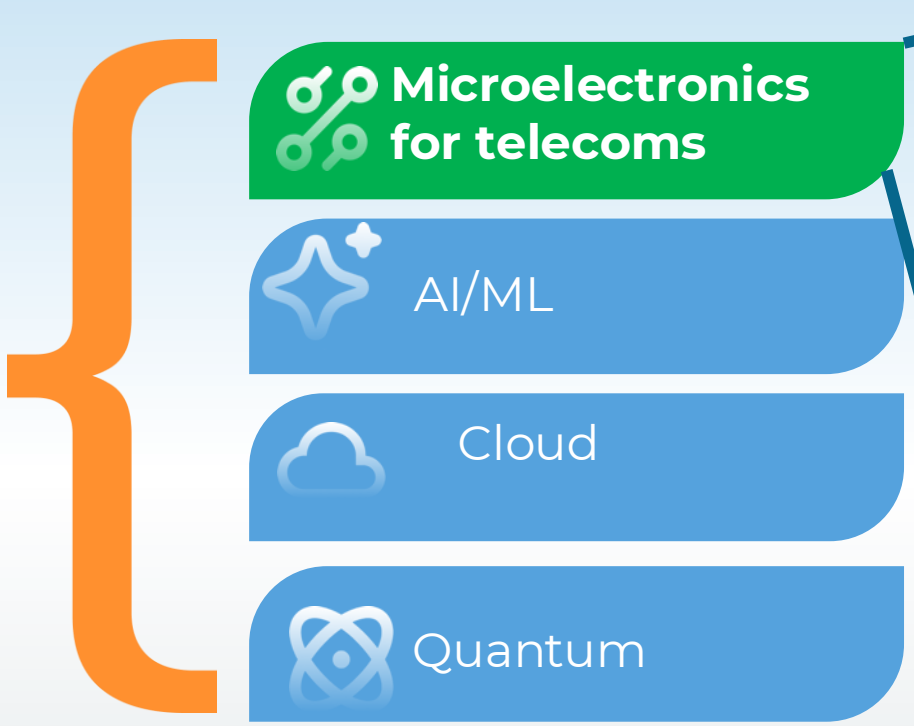
AI, Quantum, HPC, security, chipsets, computing;

The Draghi report : The telecommunication equipment and software sector are also key for the EU's cyber-resilience, security of strategic infrastructures, and protection of citizens' and business data

European Commission

Telecoms vs other key technologies

Reshape end-devices, services and connectivity



- New RF bands, beyond mmWaves
- Joint coms and sensing, dual application chipsets
- SoC's, multiple net function implementations;
- Virtualisation, HW capabilities and accelerators
- Packaging
- AI/ML, integration data management at edge and coms;
- Devices

➔ **Target expansion of EU capabilities in coms/services and µelectronics**

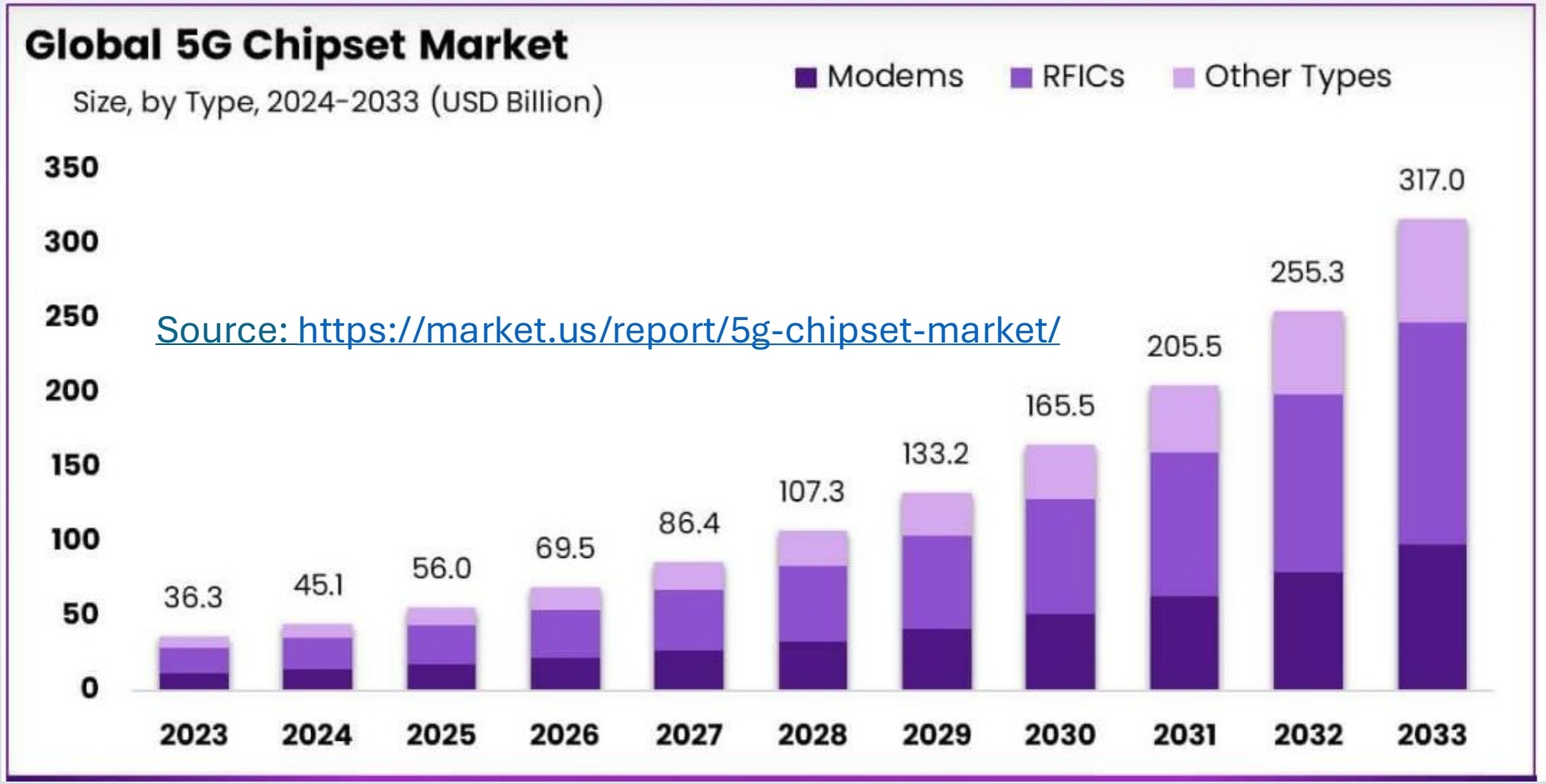
➔ **Strong ECS and SNS SRIA commonalities to build the case**

Telecoms, a growing market for chips industry

CAGR: 24%

Target Market of proposed activities: parts of the RFIC share

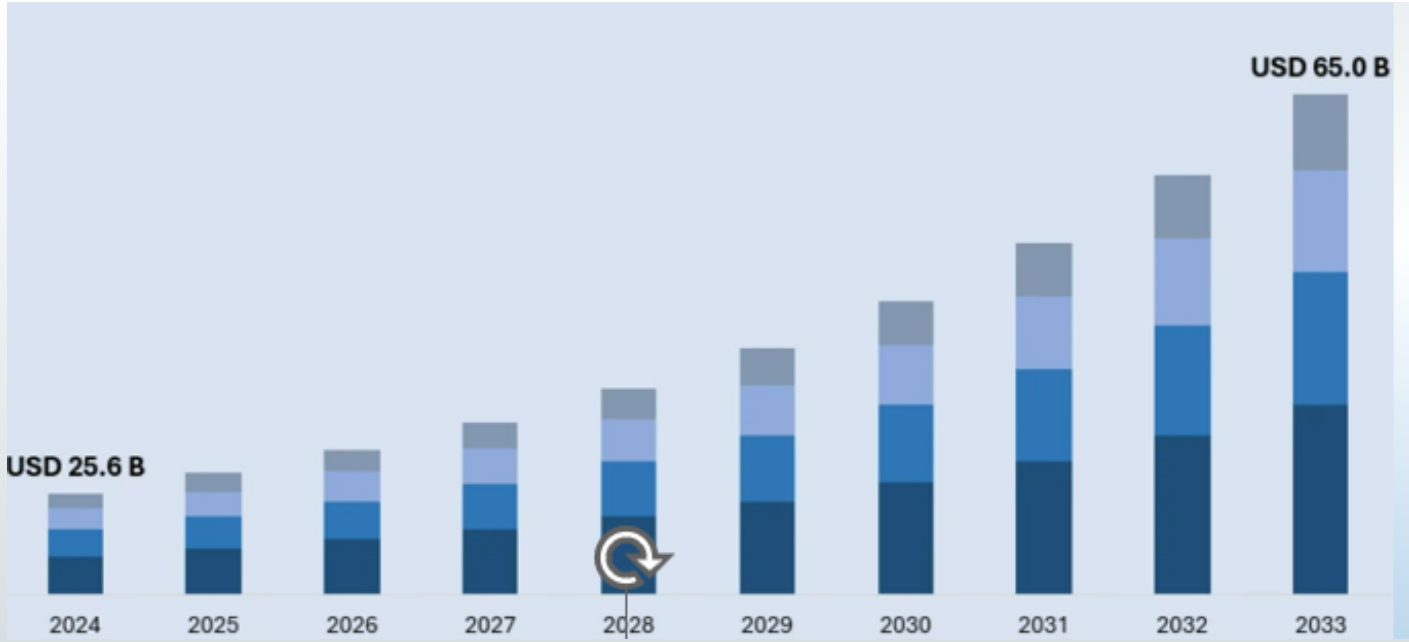
Wider market requires presence on device market



Source: https://market.us/report/5g-chipset-market/

Why a FEM proposal?

- **Multiple applications beyond Wireless Coms** ➔ (IoT, Consumer Electronics, automotive)
- **At the crossroad of EU know how, m**ixes up several strongholds: RF tech, high power tech, digital. Integration/packaging is less of an EU expertise ➔ gain knowledge in SoC design and developments
- **Pilot Lines and Chips JU, long-term planning required.**



Source: iMARC

Info day
Chips JU 6G FEM Call

HORIZON-JU-Chips-2026-2-RIA

Francisco Ignacio Serradilla
Chips JU Office

02 July 2026

EUROPEAN PARTNERSHIP

About Chips JU

- Chips JU is a tri-partite public-private partnership, established in 2023, as a successor to Key Digital Technologies JU (KDT JU) to advance nano-electronic chip technologies in Europe
- Funded by the European Union, Participating States, and Private Members

Private Members
Industry Associations

European Union
European Commission

Public Authorities
Participating States

CHIPS JU Objectives

- Contribute to the European “Leadership in Enabling and Industrial Technologies” by helping to develop a **strong and competitive ECS industry** in the Union
- Ensure ECS availability for key markets and societal challenges
  - keep Europe at the forefront of the technology development. Strategic vision. SRIA
  - **bridge the gap between research and exploitation,**
  - strengthen innovation capabilities and create economic and employment growth in the Union
- **Union of resources. HE, DEP, MS. Align strategies with Member States**, attract private investment, avoiding unnecessary duplication and fragmentation, and ease participation
- Maintain and grow semiconductor and smart system **manufacturing capability** in Europe, including leadership in manufacturing equipment and materials processing

ECS R&I Calls

Innovation along the entire value chain

- Focus topics covering AI, cybersecurity, high-performance computing (HPC), semiconductors, and more.
- Chips Joint Undertaking is aligning global research initiatives with European priorities.
- Chips JU is bridging together industry, academia, and policymakers for impactful results.
- It enables large-scale projects with EU and international investment.
- € **1.3 billion**

The Chips Act: Europe's Lifeline

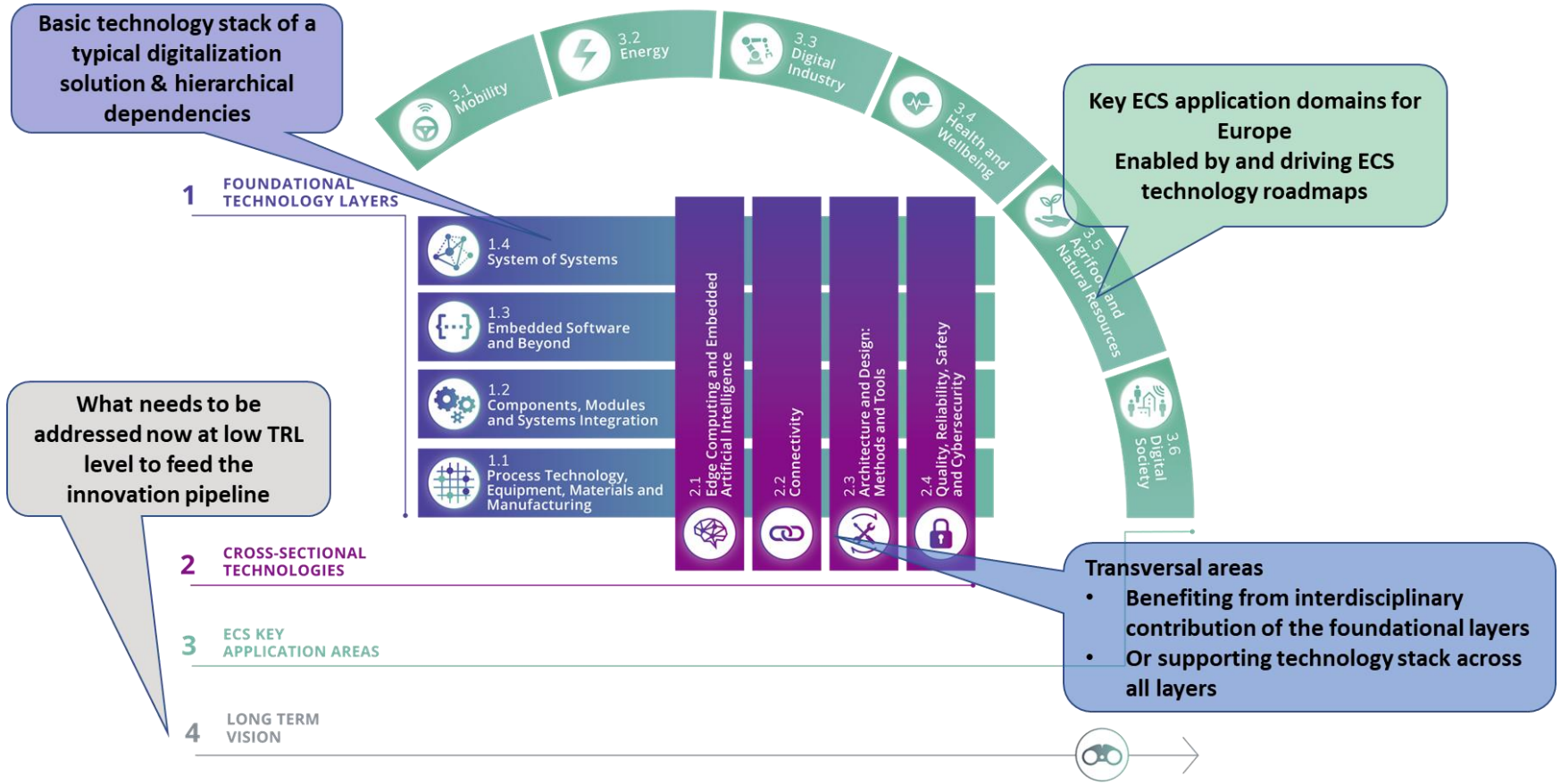
Capacity Building through the Chips Act

- **Chips Act:** one of Europe's largest industrial policies aimed at increasing Europe's share of global chip production.
- Chips JU implements the main part of the first pillar of the Chips Act, the **Chips for Europe Initiative**.
- Chips JU acts as a facilitator for public-private partnerships, ensuring that the necessary funding is directed toward strategic projects.
- It aligns the goals of the EU, its Member States, and the private sector. This **tri-partite structure** enables coordinated efforts in semiconductor innovation and capacity building in Europe.
- € **2.8 billion**

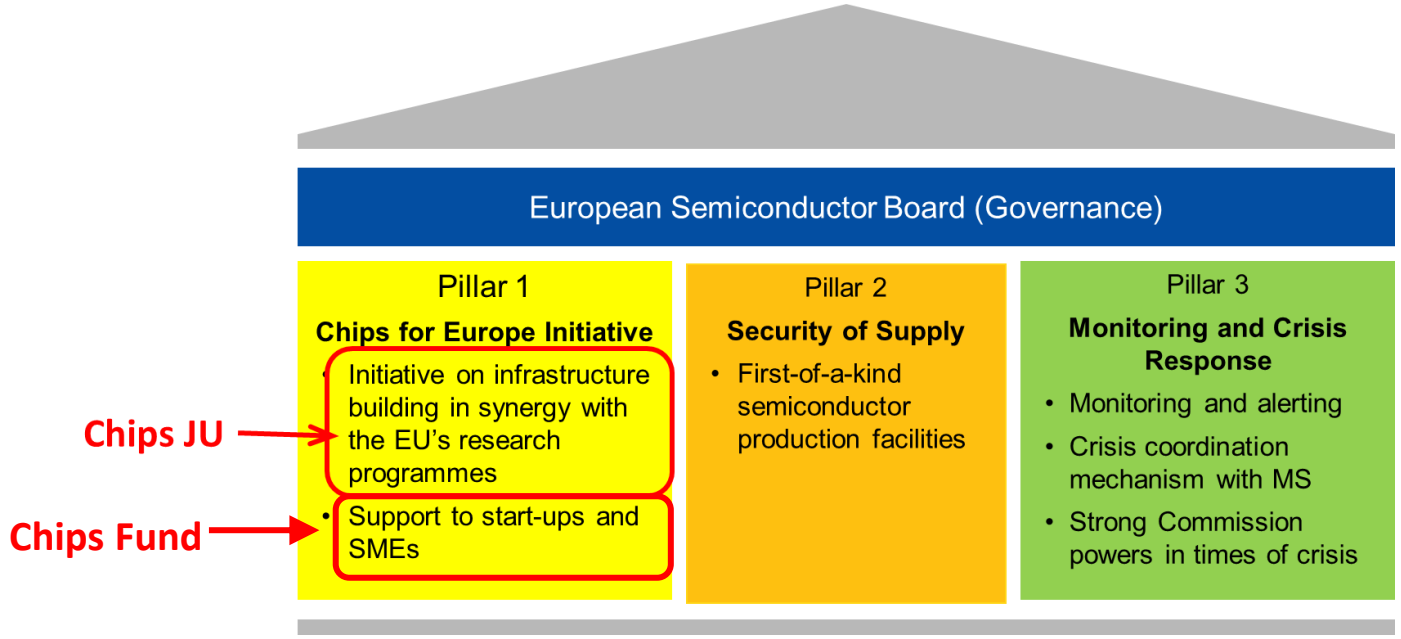
EUROPEAN PARTNERSHIP

ECS Calls: SRIA

- Boost **industrial competitiveness** through **interdisciplinary** technology innovations
- Ensure/reinforce **EU strategic autonomy** through secure, safe and reliable ECS supporting key European application domains
- Establish and strengthen sustainable and resilient ECS value chains supporting the **Green Deal**
- Unleash the full potential of intelligent and autonomous ECS-based systems for the **European digital era**



Pillar 1: Chips for Europe Initiative



- Europe is strong in R&D, RTOs and manufacturing equipment
- R&D strongly supported by MS

What is missing?

- Translating R&D into new markets
- Need for accesible infrastructure that provides advanced technologies
- Need for design capacity for those advanced technologies
- Need for workforce development
- Funding for start ups to access advanced technologies and cover scale up to manufacturing

Chips for Europe Initiative

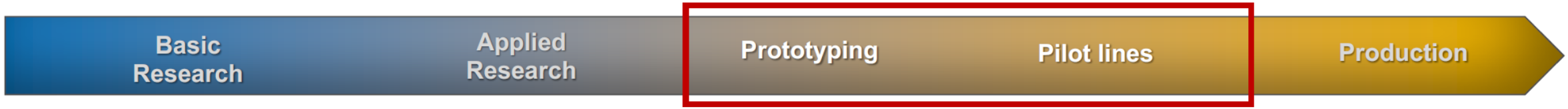
Bringing the gap from lab to fab

5 Objectives

1. Reinforce design capacity by providing a **virtual design platform**
2. Enhance existing and developing new **pilot lines**
3. Accelerate the development of **quantum chips**
4. Expand **skills** and set up a network of **competence centres**
5. Facilitate SME access to **equity and loans** through a dedicated **Chips Fund**

Chips JU

EIC
I-EU



European Commission

Bottom up versus Top down - EU versus national synergies

FOCUS TOPICS

Special topics, special calls, nudges, % of budget, special criteria (national), …

Selection taking into account national synergies

SRIA as basis for WP, consortia building, support by associations, topic selection

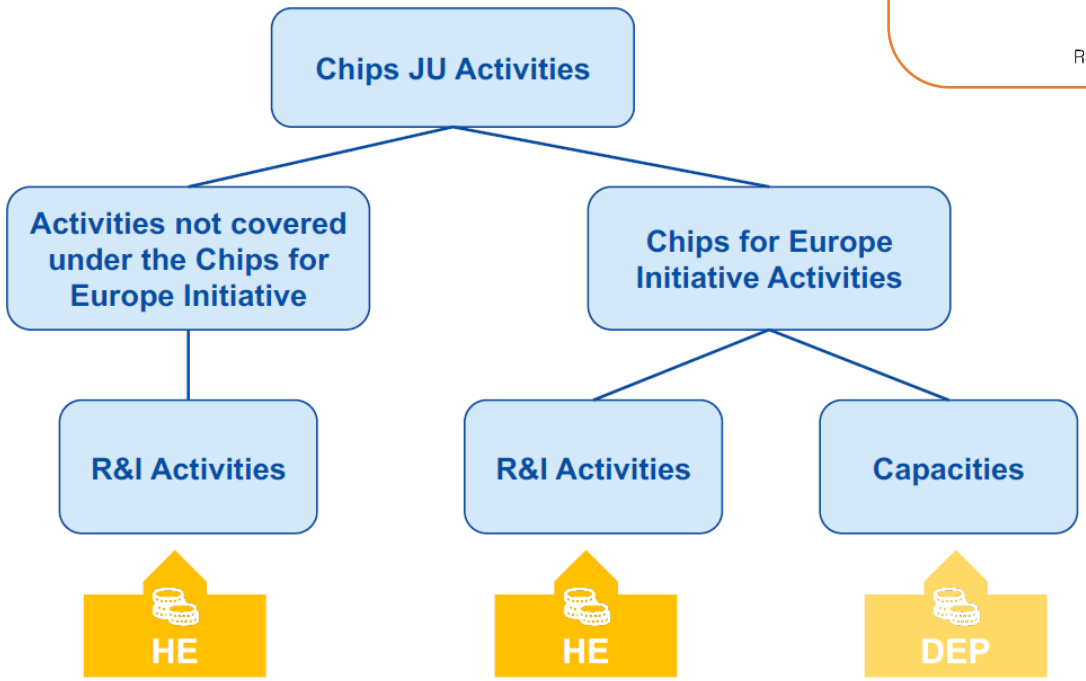
Proposals submitted by the community in regular calls for all open topics

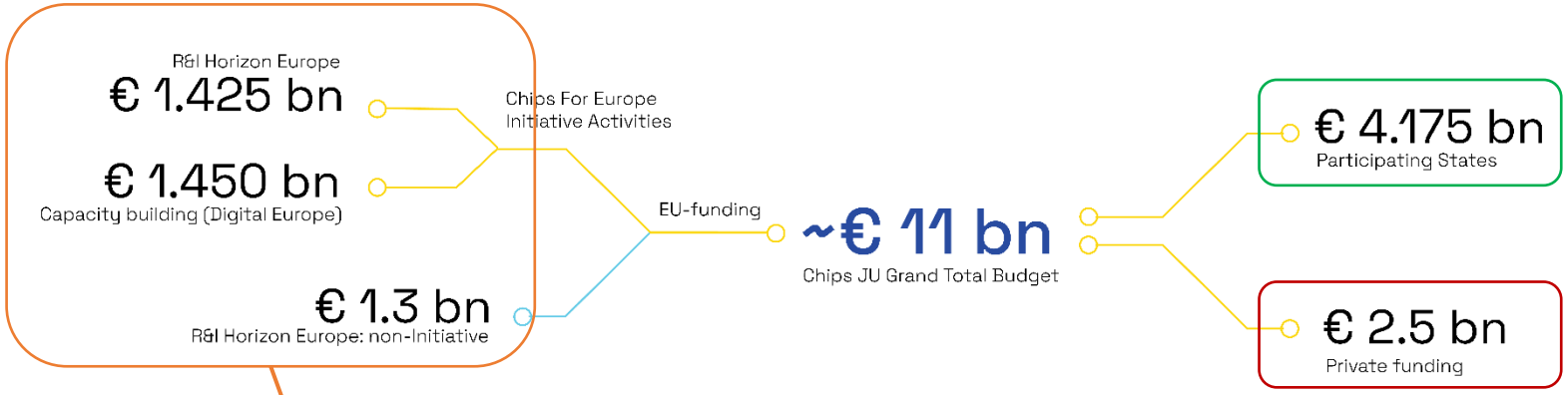
GB, WP @ or before launch

PAB @ selection

Portfolio of projects

Chips JU





EU Contribution to Chips JU (excl	Chips for Europe Initiative	Non-Initiative	Total
R&I (Horizon Europe)	1.425	1.300	2.725
Cap building (DEP)	1.450	n.a.	1.450
Total	**2.875**	**1.300**	**4.175**

Call 6G Front End Module

HORIZON-JU-Chips-2026-2-RIA

- Context
- Expected outcomes
- Scope
- Call conditions
- Budget

Context

Developing the FEM is critical for the competitiveness of European suppliers, but there are a multiplicity of **technological challenges**:

Enable **extreme massive MIMO AAS** in a compact form factor.

The increase of **antenna elements (>1000)**: requires an increase of **RF processing capability.**

The front-end IC should support **6G use cases**, which calls for a highly reconfigurable front-end solution and chiplet solutions that cover a multiplicity of functions and require integration in a SiP with advanced packaging requirements

Context

Chips Call

Address main **building blocks** of a FEM with heterogenous technologies integration at subsystem level, preparing the future complete system validation

Close aligning with the work in SNS. Collaboration between the two consortia in SNS and Chips JU calls

SNS Call

- **Design and validation** activities at Tx/Rx level, addressing use cases SBFD/ISAC and HBF/TDD
- **Validation** of technological **building blocks, system integration** and evaluation of an AAS demonstrator

Expected outcomes

Main outcome: Design/specification and implementation/testing of the key microelectronics **building blocks** of a FR3 FEM, towards a future complete integrated FEM system.

These building blocks will:

- Optimise cost-performance trade-off,
- Allow operational implementation of spectrum sharing within FR3 FEM
- Enable large arrays integration, high bandwidth for carrier aggregation with broadband RF transceivers, SBFD, ISAC

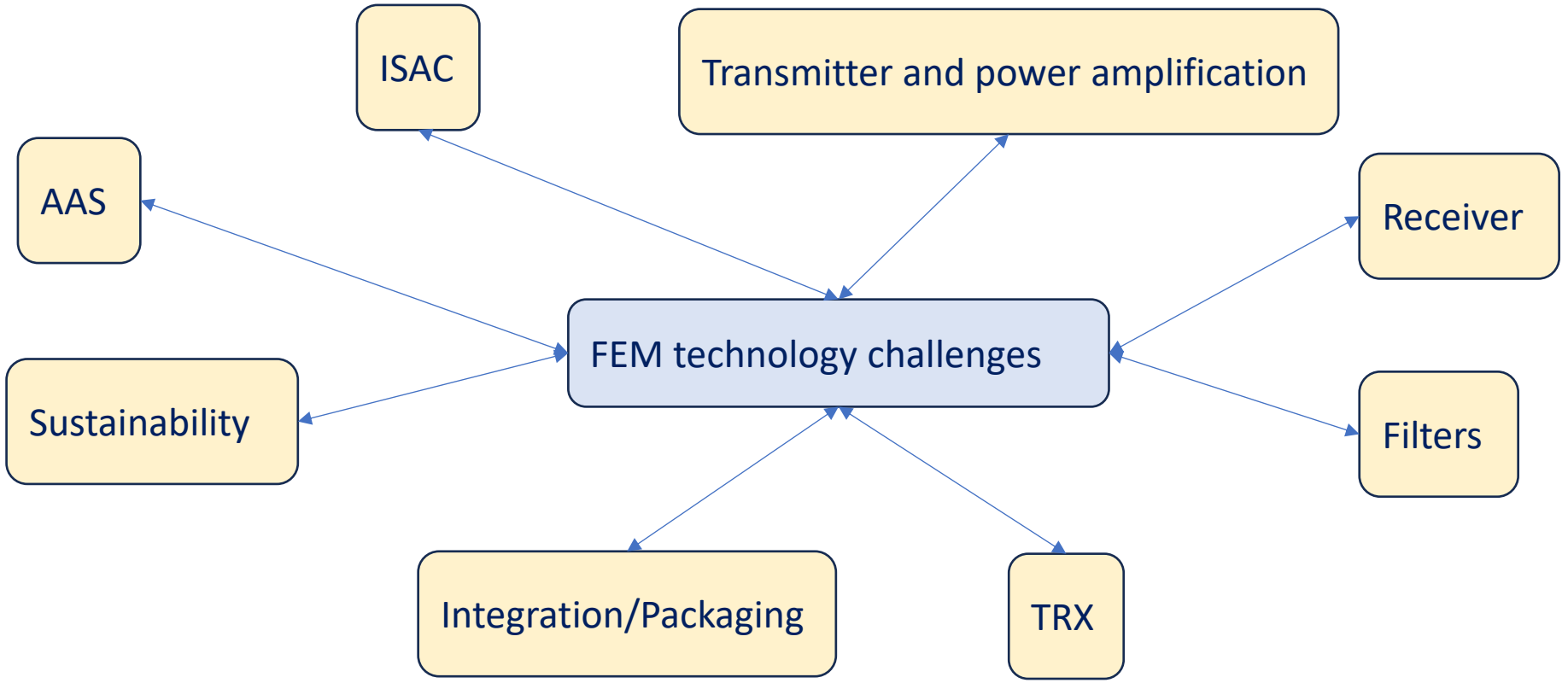
Expected outcomes

Main outcome: Design/specification and implementation/testing of the key microelectronics building blocks of a FR3 FEM, towards a future complete integrated FEM system.

- Build up on core technologies and IP blocks for further package integration and base die development for implementation of most critical functions and subsystem integration for future complete integration and verification on real environment.
- Stimulates related progress on design tools, for PDKs.
- Create synergies with the FEM project of SNS, reinforce European ecosystem of microelectronics suppliers for telecom industry, collaboration with relevant Pilot Lines is encouraged.

Scope

Proposals submitted to this call should address the following set of FEM constituent technologies in priority including challenges issues such as:



Scope

Design environment compatible with FEM technologies at TRL 5/6, development tools (PDKs) at TRL 7/8

Research on the blocks until more integration level, at least until subsystem TRL ~ 5

IP blocks expected at TRL ~ 3, with lab maturity

- Purely pre/competitive, but with clear perspective towards eventual commercialization by EU industry
- Proposals should include focused and measurable objectives and exploitation plan. Also explanation on how they plan to coordinate the activities with the SNS FEM call to contribute to the final system integration/validation levels 7/8

Call Conditions

Admissibility:

Admissibility conditions are described in Annex 1 to the multiannual work programme 2023-2027 “HORIZON Europe conditions applicable to the Chips JU” (General Annexes).

Chapter	FPP Stage
Excellence	60 pages
Impact	80 pages
Quality and efficiency of the Implementation	80 pages

Call Conditions

Eligibility:

Eligibility conditions are described in Annex 1 to the multiannual work programme 2023-2027 “HORIZON Europe conditions applicable to the Chips JU” (General Annexes).

Conditions	Limit
Max Contribution per partner (% of the total EU funding)	30 %

Participation is limited to legal entities established in EU Member States, EEA Countries (Iceland, Liechtenstein, and Norway), Associated Countries, OECD and Mercosur countries (see Annex 1 to the General Annexes to the multiannual work programme 2023-2027 “HORIZON Europe conditions applicable to the Chips JU”).

Call Conditions

Scores:

The scores will be given with a resolution of one decimal.
(*) threshold applies to unweighted score.
(**) the weight is only used to establish the ranking of the proposals in the FPP phase.

Criteria	Range	Weight (**)	Threshold (*)
Excellence	0-5	1.0	3
Impact	0-5	1.5	3
Quality and efficiency of the Implementation	0-5	0.7	3
Total	0-15		10

Reimbursement rate for establishing the EU contribution:

Reimbursement rates as percentages of the eligible cost according to HE.
(*) beneficiaries may ask for a lower contribution.

Type of beneficiary	Maximum EU Contribution as % of the Eligible Cost according to HE (*)
For profit organization but not an SME	25 %
SME (for profit SME)	35 %
University/Other (not for profit)	35 %

Call conditions and budget

Type of Action	Research and Innovation Action (RIA)
Indicative EU budget	20 M€
Expected EU contribution per project up to:	The JU estimates that an EU contribution of around EUR 20 million would allow these outcomes to be addressed appropriately. Nonetheless, this does not preclude submission and selection of a proposal requesting different amounts.
Mode	Co-funded with the NFA One stage Call
Call launch date	7 Jul 2026
Deadline FPP Stage	16 Sep 2026 at 17:00 Brussels Time

National budget commitments

Participating States	Global IA	IA-FT1	IA-FT2	IA-FT3	IA-FT4	Global RIA	FT2-RIA	Total (M€)	Comments
AT	3.50	1.50	1.50	0.00	1.40	2.50	1.00	**11.40**	
BE-FL	0.00	0.00	0.00	0.00	0.00	0.00	0.00	**12.00**	
CH	0.00	0.00	0.00	0.00	0.00	0.00	0.00	**6.00**	Switzerland has a total budget of 6 Mio. CHF for all 2026 calls, including ECS and CfEI.
DE	7.00	6.00	0.00	0.00	5.50	7.00	4.00	**29.50**	
DK	0.00	0.00	0.00	0.00	0.00	0.00	0.00	**7.33**	7.33 M EUR is the total national budget for the remaining Calls 2025 and both ECS and Chips for Europe Initiative Calls 2026. IFD does not fund SKILLS-PF-SG, SKILLS-HoE-SG, and AIDP-GfP
ES-AEI	0.00	0.00	0.00	0.00	0.00	0.00	0.00	**4.00**	AEI does not fund IA-FT4
FI	0.00	0.00	0.00	0.00	0.00	0.00	0.00	**11.00**	

National budget commitments

Participating States	Global IA	IA-FT1	IA-FT2	IA-FT3	IA-FT4	Global RIA	FT2-RIA	Total (M€)	Comments
FR	0.00	0.00	0.00	0.00	2.50	0.00	3.50	**15.00**	
HU	0.30	0.30	0.30	0.30	0.30	0.10	0.00	**1.60**	The budget allocated for each call is indicative and signal funding priority. Different budget requested will not be deemed ineligible. The total budget available for the 2026 calls is 2.4M
IL	0.00	0.00	0.00	0.00	0.00	0.00	0.00	**1.75**	
IT MIMIT	10.00	0.00	0.00	0.00	0.00	0.00	0.00	**10.00**	The provisional budget for ECS calls is equal to 10 M€ from MIMIT for all IA calls and 2.25 Me from MUR for all RIA calls. MUR will also provide 3.75 Me for Chips for Europe calls.
IT MUR	0.00	0.00	0.00	0.00	0.00	2.25	0.00	**2.25**	The provisional budget for ECS calls is equal to 10 M€ from MIMIT for all IA calls and 2.25 Me from MUR for all RIA calls. MUR will also provide 3.75 Me for Chips for Europe calls.
LV	0.00	0.00	0.00	0.00	0.00	0.00	0.00	**1.20**	
MT	0.00	0.00	0.00	0.00	0.00	0.00	0.00	**1.50**	

National budget commitments

Participating States	Global IA	IA-FT1	IA-FT2	IA-FT3	IA-FT4	Global RIA	FT2-RIA	Total (M€)	Comments
NL	14.00	5.00	5.00	5.00	1.00	9.00	0.00	**29.00**	€ 5,000,000 combined budget for IAFT1, IA-FT2 and IAFT3
NO	0.00	0.00	0.00	0.00	0.00	0.00	0.00	**2.00**	
PL	0.00	0.00	0.00	0.00	0.00	0.00	0.00	**5.50**	
PT	0.00	0.00	0.00	0.00	0.00	0.00	0.00	**3.50**	
SE	1.87	0.65	0.47	0.00	0.82	1.68	1.40	**6.90**	
SI	0.00	0.00	0.00	0.00	0.00	0.00	0.00	**0.20**	The figures provided represent the budget for all Chips Joint Undertaking calls for proposals for the period 2026–2030. The exact amounts are still subject to approval by the management and may change
SK	0.00	0.00	0.00	0.00	0.00	0.00	0.00	**0.80**	800,000 EUR allocated for LFA (2025), ECS and Chips For Europe
TR	0.00	0.00	0.00	0.00	0.00	0.00	0.00	**6.00**	
UK	0.00	0.00	0.00	0.00	0.00	0.00	0.00	**10.00**	The amount is in GBP

Thank you!