Skills Info Sessions

Matei Arghirescu, Programme Officer

June 18, 2026

Co-funded by
the European Union

EUROPEAN
PARTNERSHIP

Hubs of Excellence

DIGITAL-JU-CHIPS-2026-SKILLS-HoE-SG

€20M
Total EU budget

€4M
Estimated per project

50%
EU funding rate

Co-funded with the NFAs.

OPENS
7 July 2026

CLOSES
24 Sept 2026, 17:00
Brussels time

ELIGIBILITY ASPECTS

Participation restrictions for the protection of European digital infrastructures, communication and information systems, and related supply chains.

Ownership control: legal entities that are established in EU Member States, EEA countries (Iceland, Liechtenstein, and Norway), but are controlled from third countries may only participate on the condition that they guarantee the protection of the essential security interests of the Union and the Member States and that they ensure the protection of classified documents information.

Hubs of Excellence

Educational programs which aim to increase quality and quantity of highly specialized students by shortening the time to equip graduated for the work role.

5+ years
minimum duration

Shall focus on only one of the following areas deemed crucial for European industry:

a)

Chip design and tools for chip design

b)

Chip manufacturing, equipment metrology and testing

c)

Chiplets, heterogeneous integration, advanced packaging

d)

Technologies for photonic components and systems

e)

Power electronics and wide bandgap materials

Hubs of Excellence

Outcomes

- Long-term hubs for education that will increase the number and enhance the knowledge of specialists in semiconductor technology area.
- Increase the inflow of students in these interest areas.
- Increase the mobility of students and specialists.
- Not duplicate existing initiatives but complement them, build upon existing workforce intelligence.

Scope

- Creation of a hub specialised in one of the interest areas.
- Design of educational programs, aligning academic programmes with industry.
- Access to modern infrastructure/equipment for the specialised students.
- Intra-EU mobility, cross-border and inter-regional collaboration; suggestion to involve organizations from countries with talent surplus and talent shortages.
- Attracting talent from outside EU.
- Raising awareness, show the diversity of careers, establish career-orientation platform in micro-electronics.
- Clear KPIs.

Pilot Federation

DIGITAL-JU-CHIPS-2026-SKILLS-PF-SG

€10M	€10M	50%	5+ yrs
Total EU budget	Per proposal	EU funding rate	Min. duration

Co-funded with the NFAs.

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Pilot Federation

Outcomes

- A federation of Vocational Education and Training providers in semiconductor related technology areas.
- Reskilling programmes for professionals transitioning from other industrial sectors experiencing surplus workforce.
- Increased inflow of workers, increased intra and extra EU mobility.
- Standardized curricula for technicians and recognized certifications across the EU.

Scope

- Manage and ease mutual recognition of international systems for training, qualification and certification for technicians in the semiconductor sector.
- Provide a comprehensive overview of the European providers and of their micro-credentials offer.
- Industry-aligned micro-credentials.
- Intra-EU mobility, cross-border and inter-regional collaboration.
- Attracting talent from outside EU.
- Clear KPIs.

Stimulation of Chip Design

DIGITAL-JU-CHIPS-2026-SKILLS-SCD-CSA

€15M
EU budget

100%
EU funded

60%
to student tape-outs

4 yrs
Project duration

OPENS
7 July 2026

CLOSES
24 Sept 2026, 17:00
Brussels time

ELIGIBILITY ASPECTS

Participation restrictions for the protection of European digital infrastructures, communication and information systems, and related supply chains.

Stimulation of Chip Design

- The topic might be amended, including:
  - Some changes in scope/expected outcomes;
  - Maximum consortium size: 12 (indicative value, may be exceeded with a proper justification);
  - Ownership control restrictions (like in the other two topics).

- https://www.chips-ju.europa.eu/
  - Check the soon to be updated Work Programme (Appendix 8)

Tyndall

Planning for Hubs of Excellence Call Topic

Dr. Cian Ó Murchú
Head of EU and Strategic Programmes
Tyndall National Institute, Cork, Ireland

18th June 2026

UCC
Coláiste na hOllscoile Corcaigh
University College Cork, Ireland

Rialtas na hÉireann
Government of Ireland
Tionscadal Éireann
Project Ireland 2040
Ireland's European Structural and Investment Funds Programmes 2014-2020
Co-funded by the Irish Government and the European Union
European Union
European Structural and Investment Funds

Skills Workshop/matchmaking @EPoSS AF 2026

Skills Workshop

Cian Ó Murchú

16/06/26

Tyndall

Skills Hubs of Excellence
Topic: DIGITAL-JU-CHIPS-2026 -SKILLS-HoE-SG

Topic	Interests
Chip design and tools for chip design	3 RTOs, 2 Industry
Chip manufacturing, equipment metrology and testing	2 Industry, 1 RTO
Chiplets, heterogeneous integration, advanced packaging	3 Industry, 1 RTO
Technologies for photonic components and systems	3 RTOs, 2 Industry
Power electronics and wide bandgap materials	2 RTOs, 2 Industry

Countries: Ireland, Portugal, Spain, Austria

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Initial Ideas

- **European Joint Master's Programme** delivered through a consortium of multiple universities.
- **Industrial PhD Academy** to train doctoral candidates in close collaboration with industry.
- **Shared semiconductor training infrastructure and mobility scheme** enabling access to specialist facilities across partner institutions.
- **MSCA collaboration** to increase projects in semiconductor applications
- **European internship network with guaranteed placements** across academic and industrial partners.
- **International talent attraction programme** targeting selected countries.
- **Women in Semiconductors initiative** to improve female participation, retention, and progression.
- **Career orientation and awareness platform** promoting semiconductor career pathways and opportunities through roadshow, ambassadors, etc.
- **Integration with Chips Competence Centres and Pilot Lines** to ensure complementarity with existing EU capabilities.
- **Skills Observatory based on workforce intelligence data** to track evolving needs and guide programme design.
- **Micro-credential framework for reskilling and upskilling** aligned with industry needs.

EU Initiatives

Funding Agency	Initiative	Focus
CHIPS ACT 1.0 Chips for Europe	National Chips Competence Centres	Provide Semiconductor related training for Organizations
	Acccess CSA	Coordinating CCC Training Activities
	CHIPS JU Calls (CforE Initiative)	Three upcoming calls on Skills
	CHIPS JU Pilot Lines	Training Courses
DG CNECT	Industrial Alliance WG on Skills	Blueprint report & Video Promotion
Digital Europe	Projects such as RESCHIP4EU, Chips of Europe, Greenchips-edu	EU projects on Semiconductor training
ERASMUS+	European Chips Skills Academy, EU Chips Diversity Alliance, Centre of Vocational Excellence (upcoming)	Training and upskilling projects
IPCEI	IPCEI ME/CT - Important Project of Common European Interest	Training activities across all projects
EIT	28DGTL (formerly EIT Digital)	Masters Programmes, Online courses…
EU	Pact for Skills / Large Scale Partnership for the Microelectronics Ecosystem	Networking and collaboration

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Other recent Initiatives:

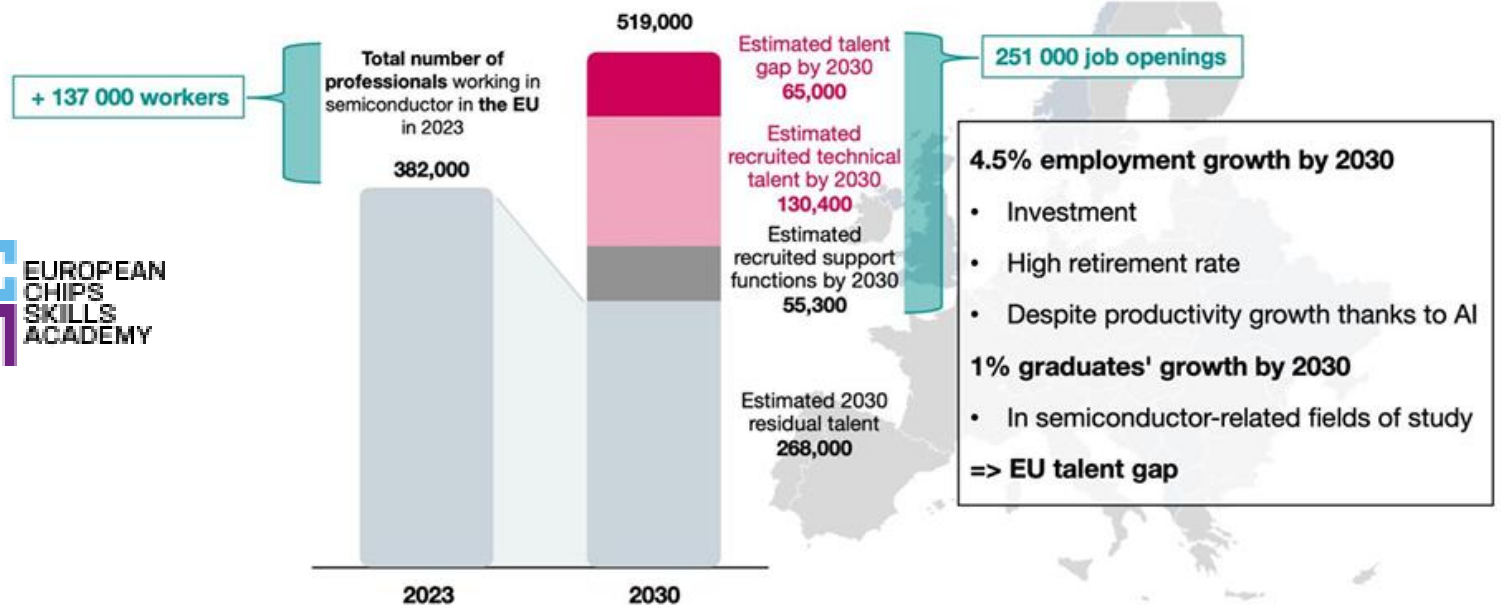
- Digital Education Action Plan 2021-2027
- European Universities Initiative
- Harnessing Talent in Europe: a new boost for EU Regions
- European Digital Innovation Hubs
- EU STEM Coalition
- Research Infrastructures (INFRACHIP, RIANA)
- A STEM Education Strategic Plan: skills for competitiveness and innovation
- CSA projects such as ICOS^2 and JASMINE

Skills Strategy Data

Figure 6: EU regions facing a talent gap versus talent surplus in semiconductor industry

EUROPEAN CHIPS SKILLS ACADEMY

Figure 5: EU Semiconductor Value Chain: Talent Gap Forecast (2024–2030)



Source: DECISION Etudes & Conseil, European Skills Strategy, ECSA, October 2025

Tyndall

Contact details

cian.omurchu@tyndall.ie

ESF

EUROPEAN SEMICONDUCTOR FEDERATION

CONNECT • TRAIN • CERTIFY • ADVANCE

CONNECTING VET PROVIDERS ACROSS EUROPE

DEVELOPING SPECIALISED TRAINING

CERTIFYING SKILLED TECHNICIANS

Problem Statement

Why a Semiconductor VET Federation?

- **Fragmentation across Europe**
  - each country and region operating its own systems, standards, and approaches, leading to inconsistencies and lack of coordination

- **Limited comparability and mobility**
  - the absence of a unified framework/body makes it difficult to compare curricula and recognise competences across borders, hindering workforce mobility and skills transfer

→ These are critical barriers which contribute to **lack of visibility** of technical career pathways, difficulty in **accessing upskilling programmes**, lack of agility to respond to **changes in labour market needs**

Needs analysis

From industry

- Challenges in **recruiting/retaining** sufficient technical talent (namely maintenance technicians, process technicians, operators)
- Significant need for **upskilling** existing workforce → evolutions in equipment, increased automation require different skillset than traditional training provides
- Need to decrease **time to work-readiness** of new graduates

From VET

- Inconsistent collaboration with industry could be harmonized, particularly when concerning **access to tools** for training
- **Lack of visibility** / attractiveness of training programs
- Differences in certification requirements can be a challenge for **curriculum updates** & cross-border mobility for students

Our ambition

Coordination

- Bringing VET into the loop, providing framework for collaboration
- Central issuing body for certification and micro-credentials

Harmonization

- What are the commonalities in training programs
- What skills are required for these job profiles

EU-level certification

- Developing a common standard for training programs
- Industry involvement in quality assurance

Upskilling

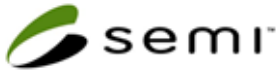
- Targeted training co-developed with industry to support continuous professional development of staff

Visibility

- Helping learners find relevant programs
- Awareness of scholarship and support opportunities for EU and non-EU students

Consortium: Current Status

Industry:



VET / Training:

What we're looking for in partners:

Areas of expertise:

- **Training delivery and design** (interpreting industry needs)
- Experience with **micro-credentials** (i.e. general knowledge, issuing, etc)
- Experience with **non-EU recruitment** campaigns
- Experience with recruiting from **underrepresented groups**
- **Main industry employers** who are experiencing shortages in this area
- **Relevant service providers** (i.e., translations, curricula design, marketing, IT)

Long-term goal: all 27 Member States represented in the Federation

Concerns & open questions

- 50% funding rate and uncertainty regarding national funding is a serious concern and a barrier to participation for some interested partners

- Can certain activities be commercialised / generate revenue? e.g., paid training programmes which issue micro-credentials

Thank you!

Anyone interested is welcome to contact me: **vcummings@semi.org**

SINANO Institute
European Academic and Scientific Association for Nanoelectronics

SiNANO plans on Skills Hubs of Excellence

June 18th, 2026

Professor Giorgos Fagas PhD MBA
Director of Strategic Development, Tyndall National Institute, Ireland
Director of SiNANO
georgios.fagas@tyndall.ie

29 members from 16 countries in Europe

SiNANO is a network of excellence connecting the European research and academic community in semiconductor science and technologies

SiNANO startup/SME community

SiNANO integrates a thriving SME community from the start-ups/spin-outs associated with our members

Our objective

To secure the future of Europe's semiconductor science and technology by

- mobilising and nurturing the European research and innovation community,
- promoting and strengthening synergies in the field through our membership,
- working with industry to accelerate innovation,
- and ensuring the growth of skilful talent in an inclusive and diverse environment with equal opportunities for all

SiNANO members' interests on skill hubs

- Chip design and tools for chip design
  - Universidad de Granada, ENSICAEN, UCLouvain, Grenoble INP, WUT/CEZAMAT, Technische Hochschule Mittelhessen, Tyndall
- Chip manufacturing, equipment metrology and testing
  - FZJ, CNRS, Universidad de Granada, ENSICAEN, University of Twente, UCLouvain, Grenoble INP, NCSR Demokritos, AMO GmbH, RWTH Aachen University, Liverpool University, Uppsala University, KTH, WUT/CEZAMAT, TU Delft, CSSNT-UPB, Tyndall
- Chiplets, heterogeneous integration, advanced packaging
  - FZJ, Universidad de Granada, ENSICAEN, BME-ETT, Grenoble INP, AMO GmbH, Uppsala University, KTH, TU Delft, CSSNT-UPB, Tyndall
- Technologies for photonic components and systems
  - FZJ, CNRS, Universidad de Granada, AMO GmbH, Grenoble INP, Liverpool University, NCSR Demokritos, TU Delft, Tyndall
- Power electronics and wide bandgap materials
  - FZJ, CNRS, Universidad de Granada, IUNET, Liverpool University, CNRS, KTH, CSSNT-UPB, Tyndall

Countries (12): Belgium, Finland, Germany, Greece, Italy, Ireland, Netherlands, Poland, Romania, Spain, Sweden, UK

Potential Coordinator

Next Steps

- Organise matchmaking among SiNANO members
- Clarify/confirm national eligibility rules

- Soliciting interest from potential industry partners

Contact: mathilde.betend@grenoble-inp.fr
georgios.fagas@tyndall.ie

Follow us:
www.sinano.eu
sinano-institute

ePIXfab

The European Silicon Photonics Alliance

Mattias Verstuyft
Director of ePIXfab
Lecturer at Ghent University

About ePIXfab

ePIXfab acts as a catalyst for European academia and industry to strengthen the worldwide silicon photonics ecosystem.

Advocate

For the promotion of silicon photonics

Represent

European silicon photonics community as a whole

Train

With respect to silicon photonics tech. & app.

Network

Connect actors in the photonics community

Mapping

Examining technology trends and anticipating future trajectories

ePIXfab timeline:
from MPW technology broker to an open alliance

2006

Silicon Photonics platform for MPW Services

imec cea leti

2015

Handover of MPW services to Europractice

EUROPRACTICE IC SERVICE

Transition to **European Silicon Photonics Alliance**

ePIXfab

2026

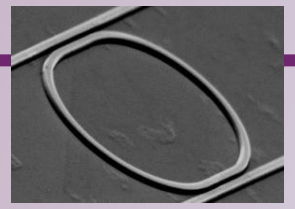
ePIXfab strengthens silicon photonics ecosystem

ePIXfab

ePIXfab members

Institute of Semiconductors CAS 1960
imec
VPIphotonics DESIGN AUTOMATION
MINISTERIO DE CIENCIA E INNOVACIÓN
CSIC
CNM Centre Nacional de Microelectrònica IMB
Politecnico di Bari
GHENT UNIVERSITY
Politecnico di Torino International University 1859
NOEIC 国家信息光电子创新中心 NATIONAL OPTOELECTRONICS INNOVATION CENTER
SANT'ANNA SCHOOL OF ADVANCED STUDIES PISA
xfab
SCINTIL PHOTONICS
DTU Fotonik Department of Photonics Engineering
DTU Technical University of Denmark
UNIVERSITAT POLITÈCNICA DE VALÈNCIA
ihp
cnit consorzio nazionale interuniversitario per le telecomunicazioni
PNTLab Photonic Networks&Technologies
iPRONICS Programmable Photonics
ZHEJIANG UNIVERSITY 1897
TNO
LUCEDA PHOTONICS
UMEC 联合微电子中心 UNITED MICROELECTRONICS CENTER
University of Southampton
leti cea tech
Tyndall National Institute Institiúid Náisiúnta | 40 years
DALIAN UNIVERSITY OF TECHNOLOGY 1949
VTT
OneTouch TECHNOLOGY BV
SITRI 上海工研院 SIMIC HOLDINGS
RWTH AACHEN UNIVERSITY
TU/e EINDHOVEN UNIVERSITY OF TECHNOLOGY
合肥华宇半导体 HISEMI SEMICON
epiphany
KAIST
SiPhotonIC TECHNOLOGIES
Technische Universität Berlin
SAL SILICON AUSTRIA LABS
LIGENTEC
WinPhoS Research Group
O'Shenu
ST
BRIGHT Integrated PHOTONICS
VLC PHOTONICS A Hitachi Group Company
AMO
C2N
LioniX INTERNATIONAL

Photonics Research Group





- Research Group of Ghent University
  - Faculty of Engineering and Architecture
  - Department of Information Technology (INTEC)
  - Associated laboratory of IMEC
  - Member of the Center for Nano- & Biophotonics (NB photonics)
- Technology Research
  - Photonic Integrated Circuits: light on a chip
  - On silicon: “Silicon Photonics”
  - Enhanced with new materials: III-V, ferro-electrics, graphene, …
- Applications
  - High-speed telecom and datacom
  - Sensing for life sciences: visible and Mid-IR
  - Optical information processing

12 Professors

23 postdocs

70 PhD students

14 support staff

20+ nationalities

7 ERC grants

7 spin-off companies

50 journal papers/year

Class 100 clean rooms

M.Sc. Photonics program

Advanced Master Photonics program

ePIXfab

The ePIXfab team

Chair Emeritus
Roel Baets

Chair
Wim Bogaerts

Director
Mattias Verstuyft

Technical Coordinator
Sarah Masaad

Marketing &
Communication
Officer – Mingjie Li

Technical Coordinator
Antonietta Parracino

Asia Liaison
Officer
William Chen

ePIXfab

The ePIXfab Steering Board

Dr. Timo Aalto

Dr. Iñigo Artundo

Dr. Sylvie Menezo

Prof. José Capmany

Dr. Arne Leinse

Prof. Martijn Heck

ePIXfab

ePIXfab's activities

ePIXfab acts as a catalyst for European academia and industry to strengthen the worldwide silicon photonics ecosystem.

Latest advancements in the field of silicon photonics

European silicon photonics community as a whole

With respect to silicon photonics tech. & app.

Connect actors in the photonics community

Examining technology trends and anticipating future trajectories

Silicon photonics summer school

5- days | 120 Participants | Onsite

Ghent, June 2025

- Lectures from experts in the field

- Starting from the basics
  - Technologies
  - Building blocks
  - Design & Simulation
  - Packaging
  - Applications

ePIXfab

Asia-Europe Symposium and Short Course
3 days | 100 Participants

- 2 day short course in Silicon Photonics
- 1 day symposium

2023: Hangzhou (Zhejiang University)
2024: Hong Kong (Chinese University)
2025: Singapore (A*Star-IME)
2026: Bangalore

ePIXfab

Photonhub Europe experience centers

3- days | 10 Participants | Onsite

- Quick start with photonic chips
  - Make a simple chip design
  - Fabricate it with e-beam
  - Measure your own chip

A full hands-on experience.

ePIXfab

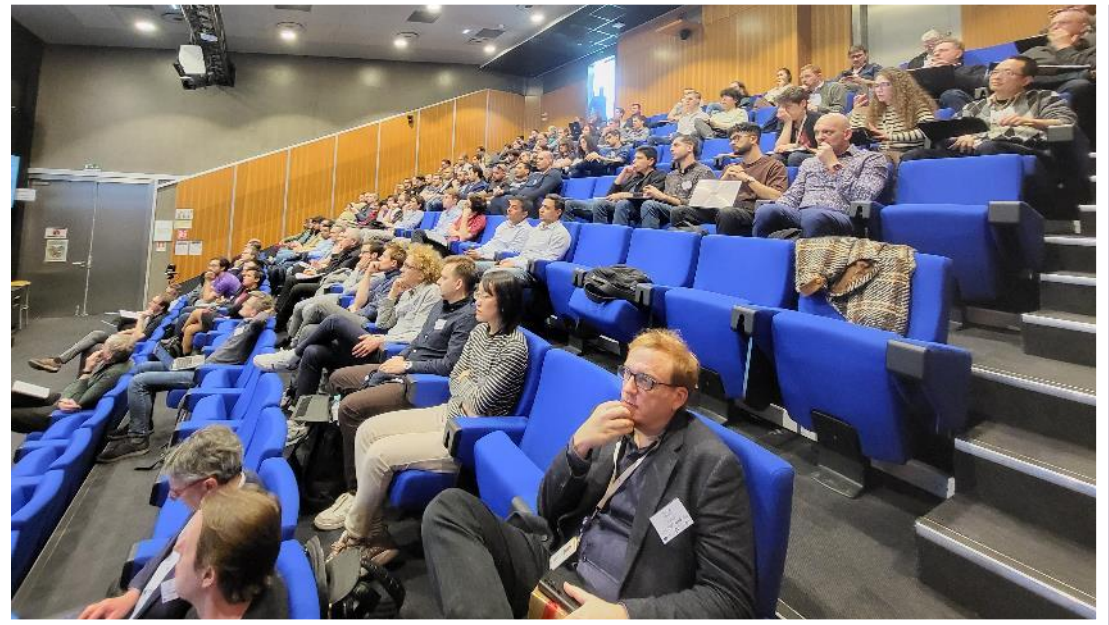
PhotonHub Europe

Cross-fertilization workshops between EU projects

2 days | 100+ Participants | On-Site + streaming

- Bring multiple projects together around a single theme
- Identify strengths, mutual interests and opportunities for collaboration
- Collocate with project meetings

- April 2024 (Thales – Paris): Heterogeneous integration
- February 2025 (Ljubljana): Photonics for Quantum
- Now: June 2026 (Ghent): High-speed optical modulators



ePIXfab

Hands-on design course in silicon photonics

5 days | 20 Participants | On-site

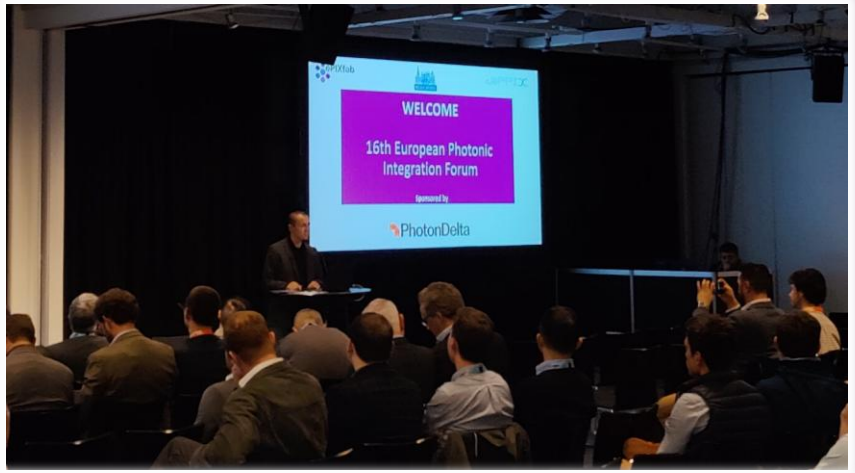
- Very intensive course
- From SiPh basics to designing your own chip
- Lectures + hands-on design labs using Jupyter notebooks
- Opportunity to have your design fabricated (passive chip with e-beam)

Next edition: April 2026

ePIXfab

European Photonic Integration Forum
2 hours | 100 Participants | at ECOC

- Organized together with JePPIX & PhotonDelta
- Interviewing two key guests
- Discussion around a hot topic for PICs



Join us in 2026 in Malaga

ePIXfab

JePPIX

PhotonDelta

Contact us for further information

Mattias.Verstuyft@UGent.be

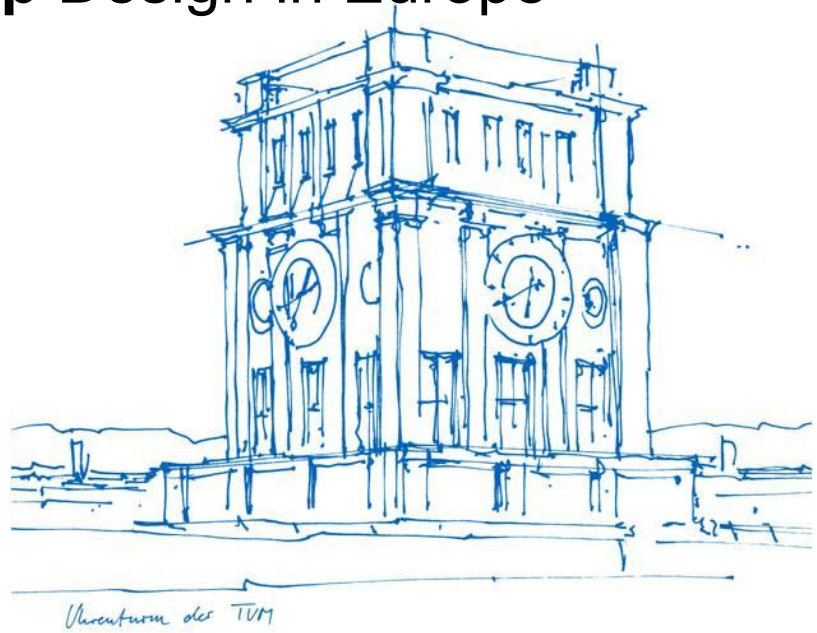
info@ePIXfab.eu

ePIXfab

Edu4Chip

Joint **Edu**cation **for** Advanced **Chip** Design in Europe

PD Dr.-Ing. habil. Michael Pehl
Chair of Security in Information Technology
TUM School of Computation, Information and Technology
Technical University of Munich
Contact: m.pehl@tum.de



Funded by the European Union

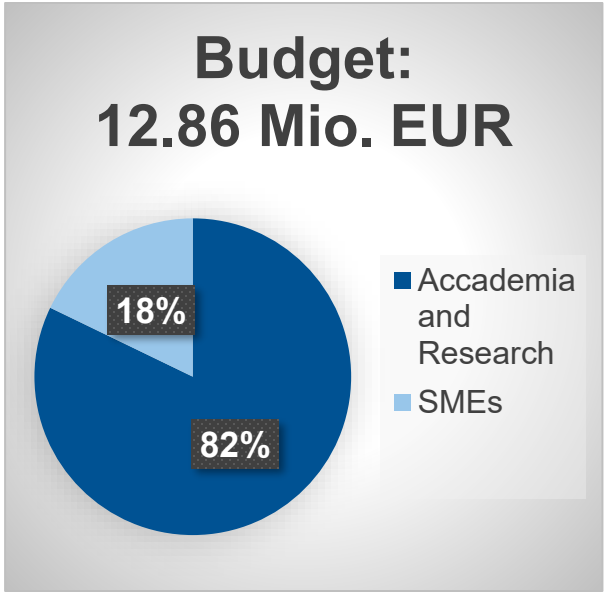
Agenda

- What is Edu4Chip?
  - Funding.
  - Partners.
  - Core Developments.

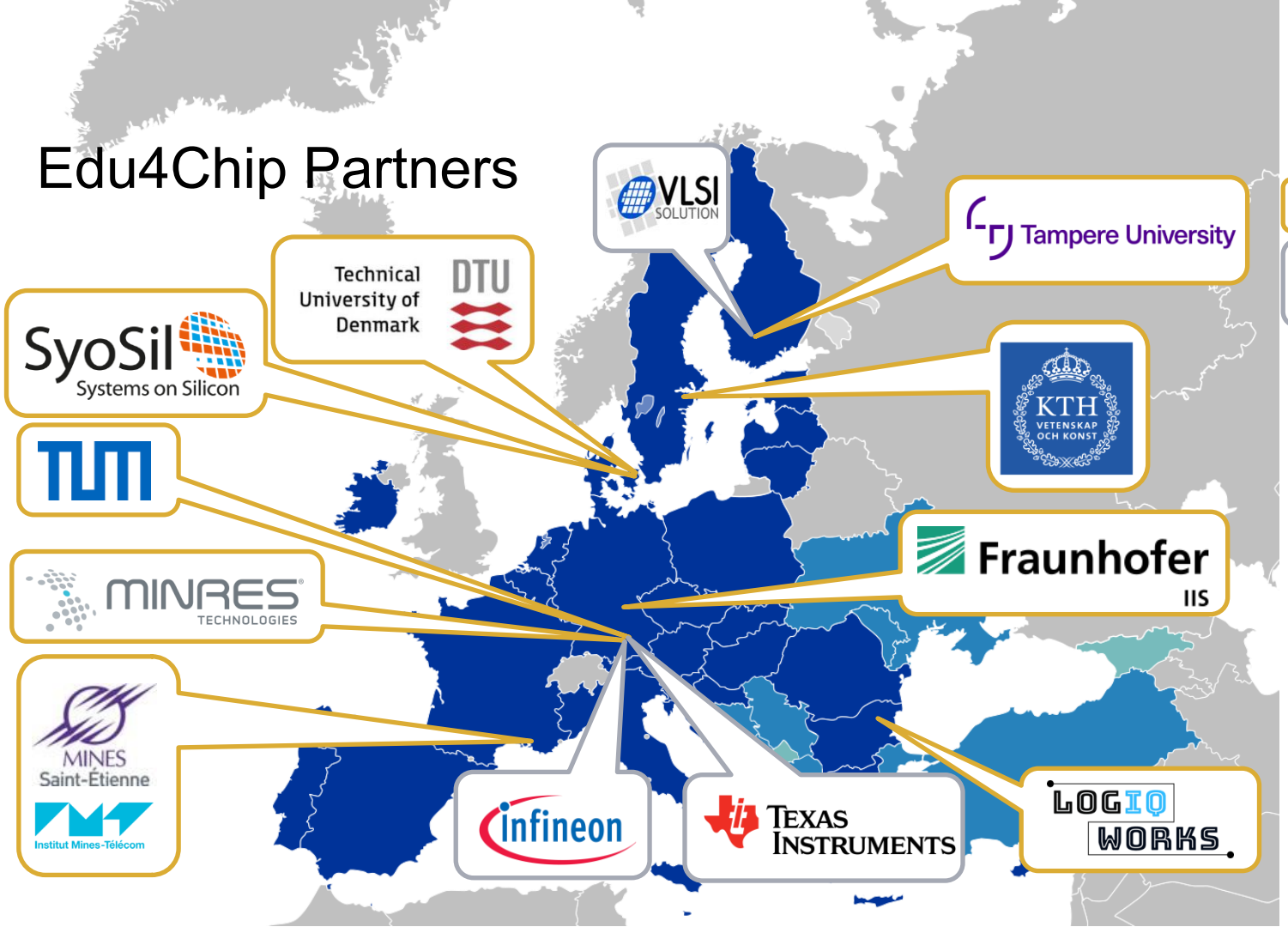
- How to make use out of it?
  - Core challenges during the setup of the project.
  - Resources offered.

Joint Education for Advanced Chip Design in Europe (Edu4Chip) – Key Data

- Call “Digital Europe Specialised Education Programmes” (DIGITAL-2022-SKILLS-03).
- 9 Beneficiaries
  - 5 universities, 3 SMEs, 1 center of excellence.
  - Project leader: TUM.
- Budget: 12.86 Mio. EUR; 50% funding.
- Project duration: October 2023 – September 2027.



Edu4Chip Partners



9 Beneficiaries

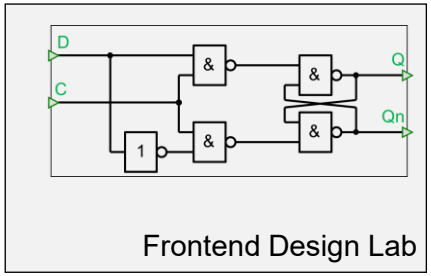
3 Associated Partners

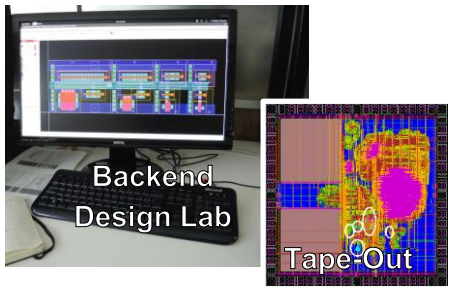
7 Supporters

- Airbus Defence and Space GmbH
- Google Germany GmbH
- Intel Deutschland GmbH
- MunEDA GmbH
- NXP Semiconductors Germany GmbH
- Robert Bosch GmbH
- Thales DIS France SAS

Edu4Chip Aligned Master Programs

Term 1	Term 2	Term 3	Term 4
Local Modules (existing/new)	Local Modules (existing/new)	Local Modules (existing/new)	Master Thesis Project
Online Modules (new/existing)	Online Modules (new/existing)	Online Modules (new/existing)	
	Development of Green Hardware	Research Internship (Industry Partner)	

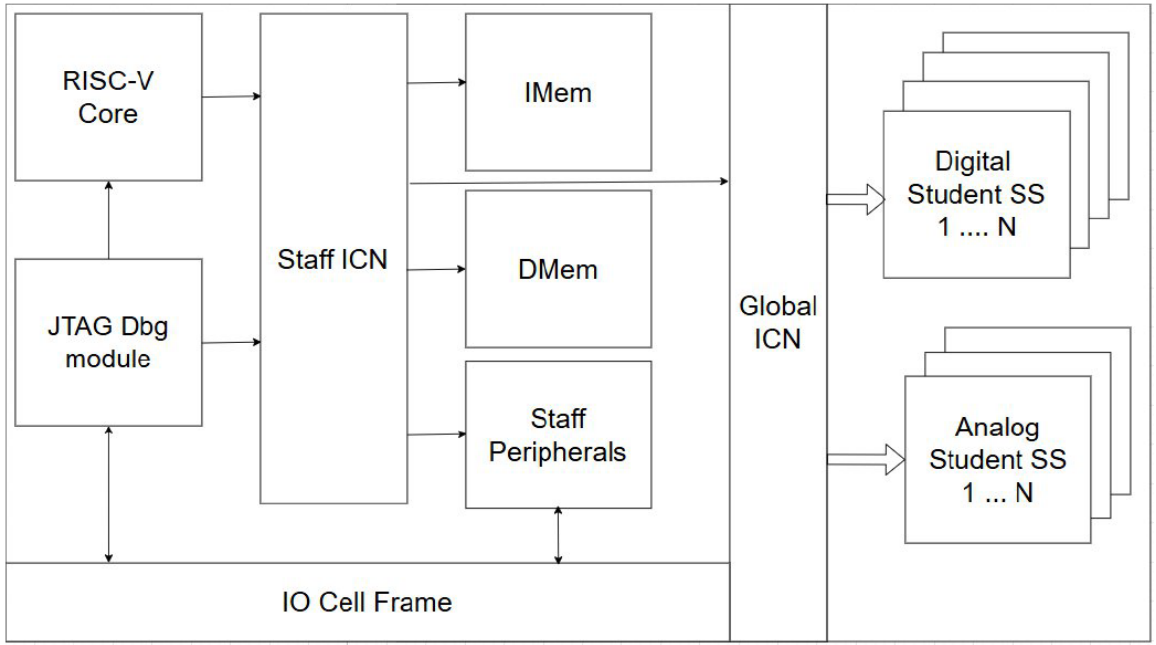




Chip Design Tape-Out Project

Life-long learning modules

Edu4Chip Didactic-SoC



- Platform for ASIC-Design by students.
- “Staff-part” ensures basic functionality.
- Students provide independent designs.

Core Challenges

- University-specific, national, European and international regulations:
  - ➢ Collaboration between countries more difficult than expected.
    Solution: Aligned programs, no joint programs/degrees, partially as separate programs or within existing programs.
  - ➢ Export control (US) and NDAs:
    - Technology access depends on nationality and
    - Students cannot be forced to sign NDAs but
    - Universities must take students independent of nationality and willingness to sign NDAs and ensure feasibility of studies.

    Solution: (i) Different tracks depending on export control status of students and
    (ii) For one partner pure open-source-based programs
- 50% funding of program
  - ➢ Co-funding (at that time) not easy to get → individual solutions per partner.

Resources

- Detailed information on the program, curricula, achievements: https://edu4chip.github.io
- Didactic-SoC: https://github.com/Edu4Chip/Didactic-SoC
- Didactic-PCB: https://github.com/Edu4Chip/Didactic_PCB
- Feel free to contact me in case of questions: m.pehl@tum.de

ODE4EC-CES
Chips for Every Student

Presentation at the Session on the Chips 2026 Calls on Skills

Stefan Wallentowitz • *Hochschule München and FOSSi Foundation*

Frank K. Gürkaynak • *ETH Zürich*

Open Design Environment for European Chips (ODE4EC) **initiative**

https://ode4ec.eu

EUROPEAN PARTNERSHIP

Vision

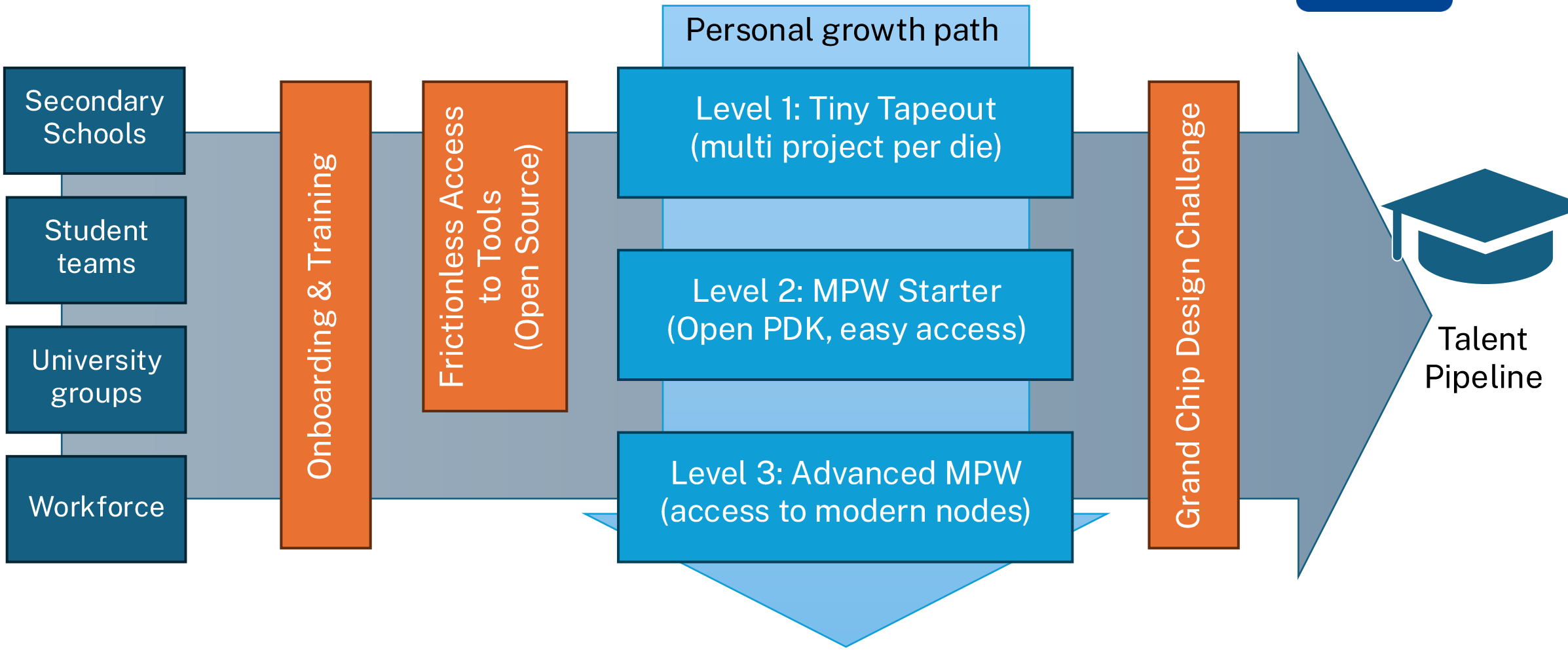
We want to widen the funnel of talent

- Universities that currently do not have IC Design experience
- Students from adjacent fields
- Reach high-school students before decision for field
- Re- and upskilling

Newcomers require ***frictionless*** access to chip design

- Base activities on open source: tools, design IP and PDKs
- Make it very easy to use, gamification
- Generate excitement, stimulate the talent pipeline

Targeting Thousands of Students



Outreach and Training

Main challenge: reaching people that will benefit

- High schools are especially challenging, need local support
- Simplify/gamify the experience to reach high school kids
- Mix of Competence Centers, groups already active in outreach
- Good geographical distribution

Key point: *frictionless* access to tools and technologies

- Can not reach 100s of universities and high schools with proprietary solutions

Still activities with proprietary solutions

- Most of Level 3 and also some at Level 2

Partner & Network Discussions

Lead

Hochschule München University of Applied Sciences

The FOSSi Foundation.

Technical Core

Fraunhofer IIS

CIME-P

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

TU/e Eindhoven University of Technology

Chips-IT

JKU Johannes Kepler Universität Linz

ihp

Network, Outreach & Training

infineon

life.augmented

semi

amu

OSRAM

GESELLSCHAFT FÜR INFORMATIK

DTU

POLITECNICO MILANO 1863

Politecnico di Torino

POLITÉCNICA

CHIPTECH TWENTE

mesap

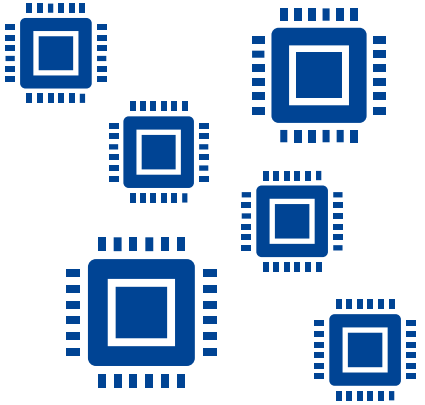
TU Graz

KIIP

INESCTEC

ODE 4 EC

More Students



More Chips

What we are looking for

Strong Technical Core Team forming already

- FTEs for key technical tasks (packaging, logistics, administration)
- Currently identifying gaps

Network, Outreach and Training

- Modest contribution to support regional activities
- Several strong partners committed
- Will grow to get better coverage across EU
- Currently strong in AT, DE, ES, FR, IT, NL
- Want to cover more countries and types

Thank you for your attention!

Get in touch!

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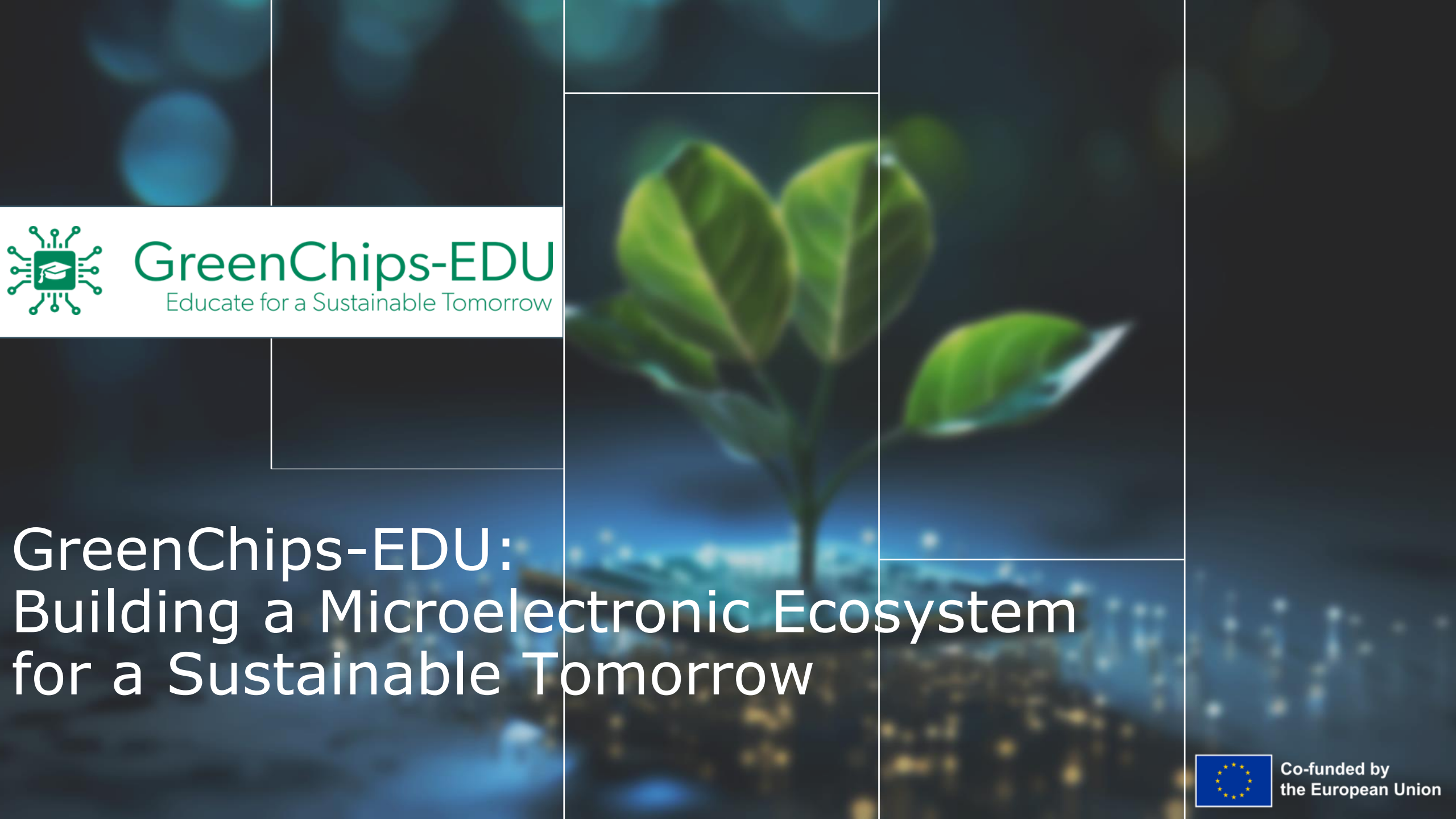
Frank Gürkaynak, kgf@ethz.ch

Open Design Environment for European Chips (ODE4EC) initiative

https://ode4ec.eu

EUROPEAN PARTNERSHIP



GreenChips-EDU
Educate for a Sustainable Tomorrow

GreenChips-EDU: Building a Microelectronic Ecosystem for a Sustainable Tomorrow

Co-funded by the European Union

About Us

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The Project at a Glance

- **Project Name: GreenChips-EDU**
  Building a Digitally-Supported Education Ecosystem for Next Generation Microelectronics Experts in Sustainable Chips and Applications for a Green and Circular Economy

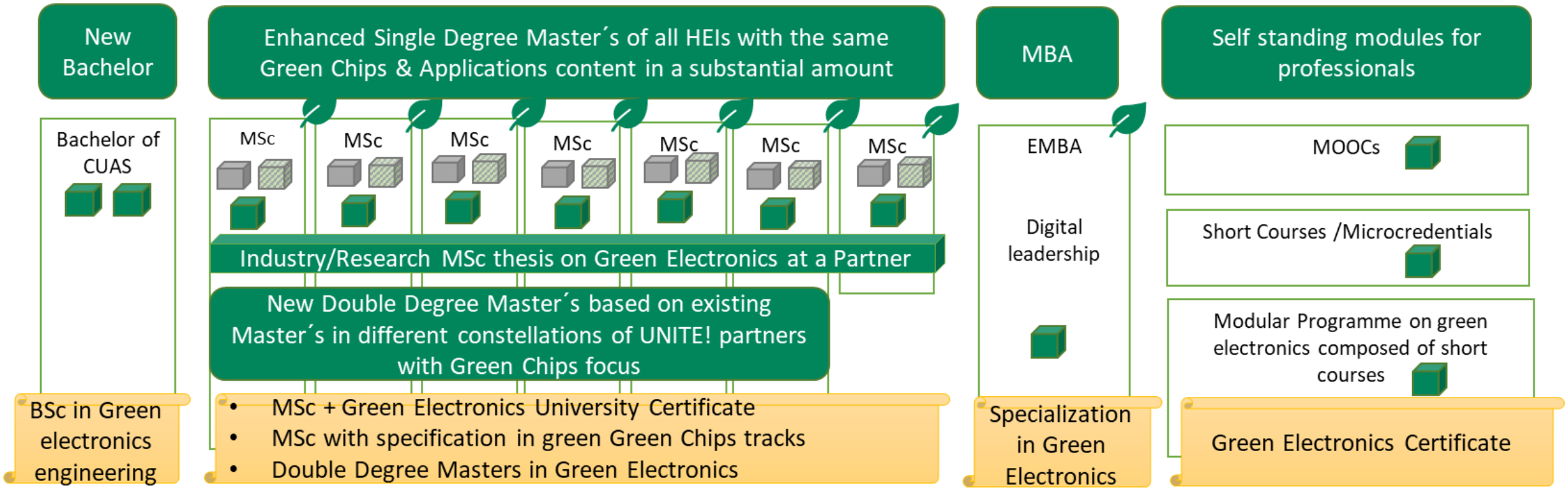
- **EU Programme:** Digital Europe Programme (DIGITAL)
- **Call:** DIGITAL-2022-SKILLS-03-SPECIALISED-EDU
- **Duration:** 48 months
- **Total budget:** 14 339 172€ **EU Funding:** 50%
- **15 key players** from **7 EU countries**,
- **6 Unite! Partners**

Motivation

- Need of **experts in green chip development**, shortage of microelectronics talent in Europe
- **Increased interest in sustainability** topics among students
- The GreenChips-EDU project addresses challenges by offering **education in both green and digital microelectronics technologies**
- Project aims at **developing expertise aligned with industry needs**

Goal: Building a digitally supported education ecosystem for microelectronics.

GreenChips-EDU Education Ecosystem



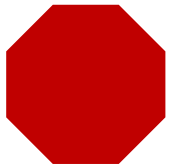
Lessons Learned

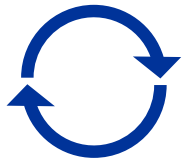
GreenChips-EDU
Educate for a Sustainable Tomorrow

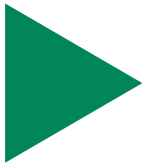
EUROPEAN CHIPS SKILLS ACADEMY

AT-C³

METIS

STOP 

CONTINUE 

START 

Lessons Learned

STOP

- Focus on rigid curricula
- Introduce static double degrees
- Focus only on technical topics

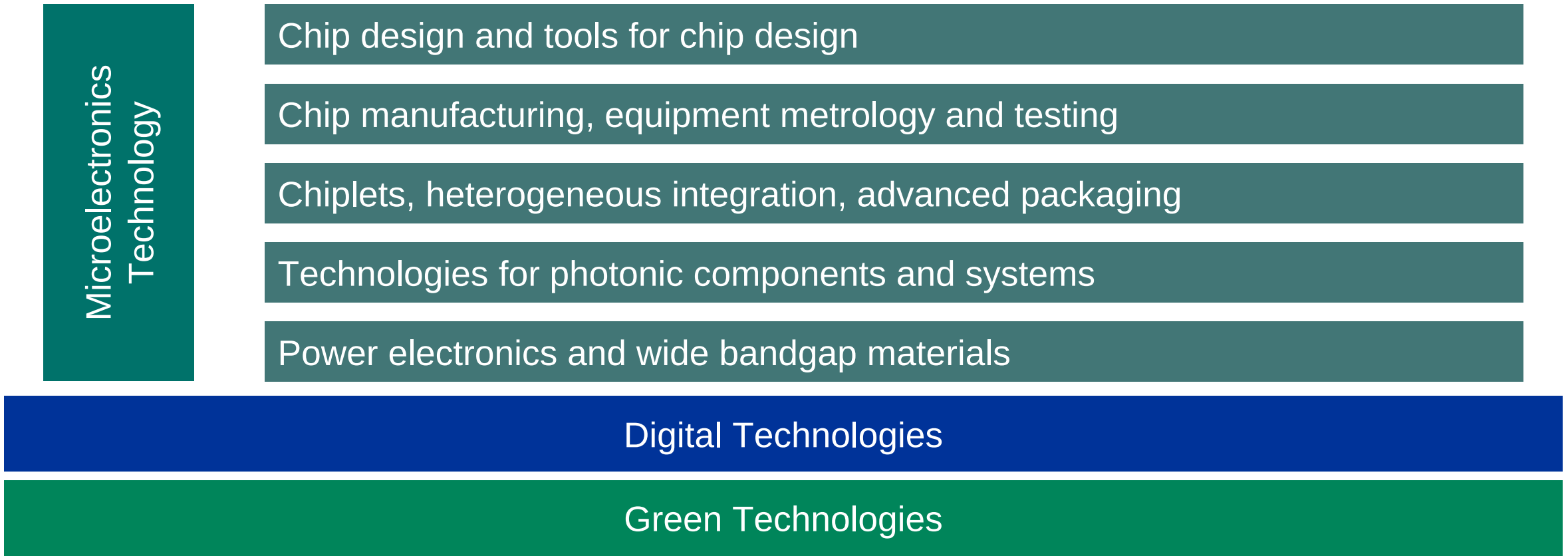
CONTINUE

- Exploit synergies on European level
- Develop shared, reusable OERs
- Focus on green transition
- Support digital literacy
- Promote an EU-wide understanding of „green microelectronics“

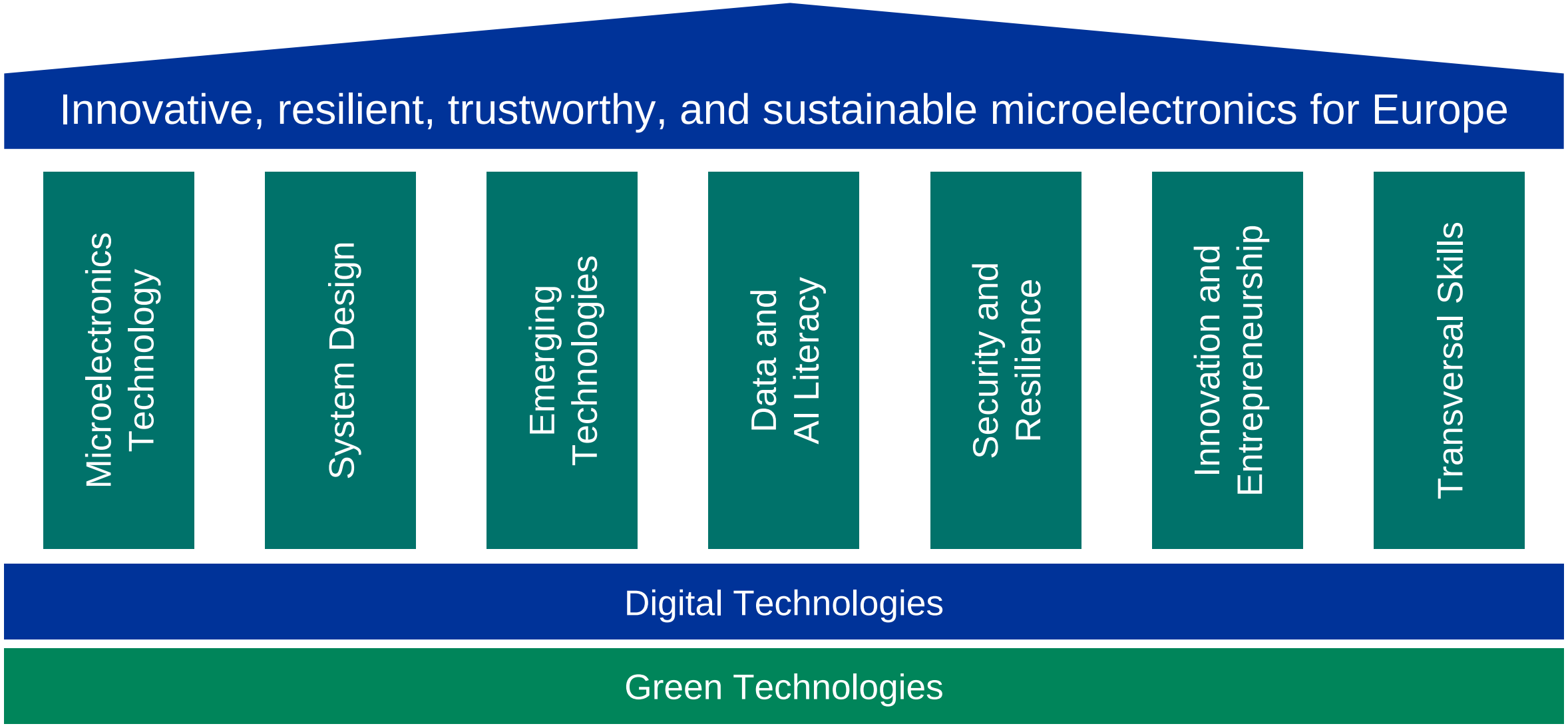
START

- Focus on emerging technologies
- Introduce innovation and business-related competences
- Introduce AI-related competences
- Define competence-based curricula
- Develop modular and accessible learning and recognition
- Treat OERs as long-term infrastructure
- Reduce fragmentation

Future of Microelectronics Education?



Future of Microelectronics Education?



Contact and Further Information

GreenChips-EDU
Educate for a Sustainable Tomorrow

https://www.greenchips-edu.eu/

AT-C3

https://atc3.at/

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